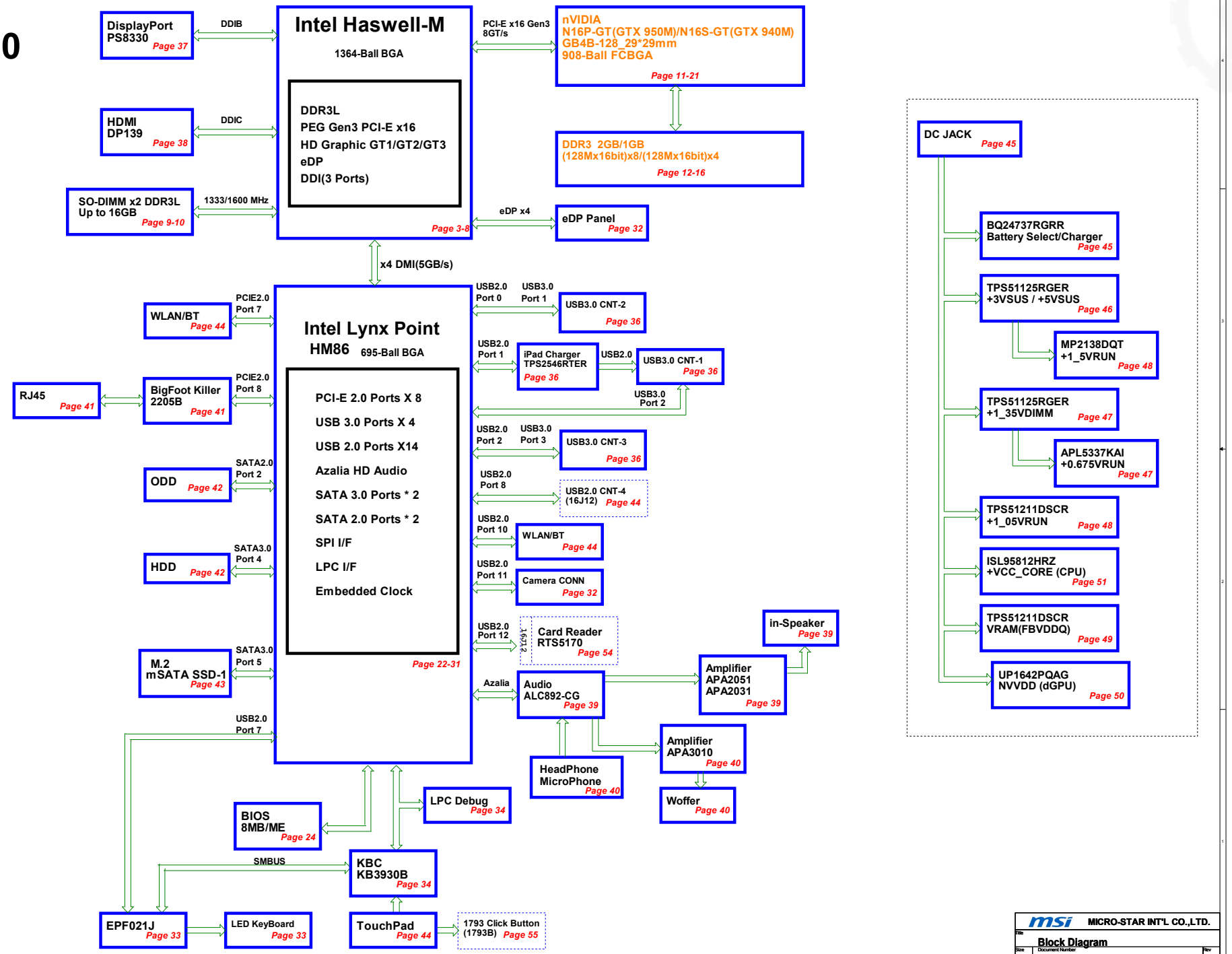
MS-16J3/MS-1793

Ver:1.0

Shark Bay Mobile



msi	MICRO-STAR INT'L CO.,LTD.
Title	Block Diagram
Size	Document Number: MS-16J2
Rev	1.0
Date:	Sheet 1 of 60

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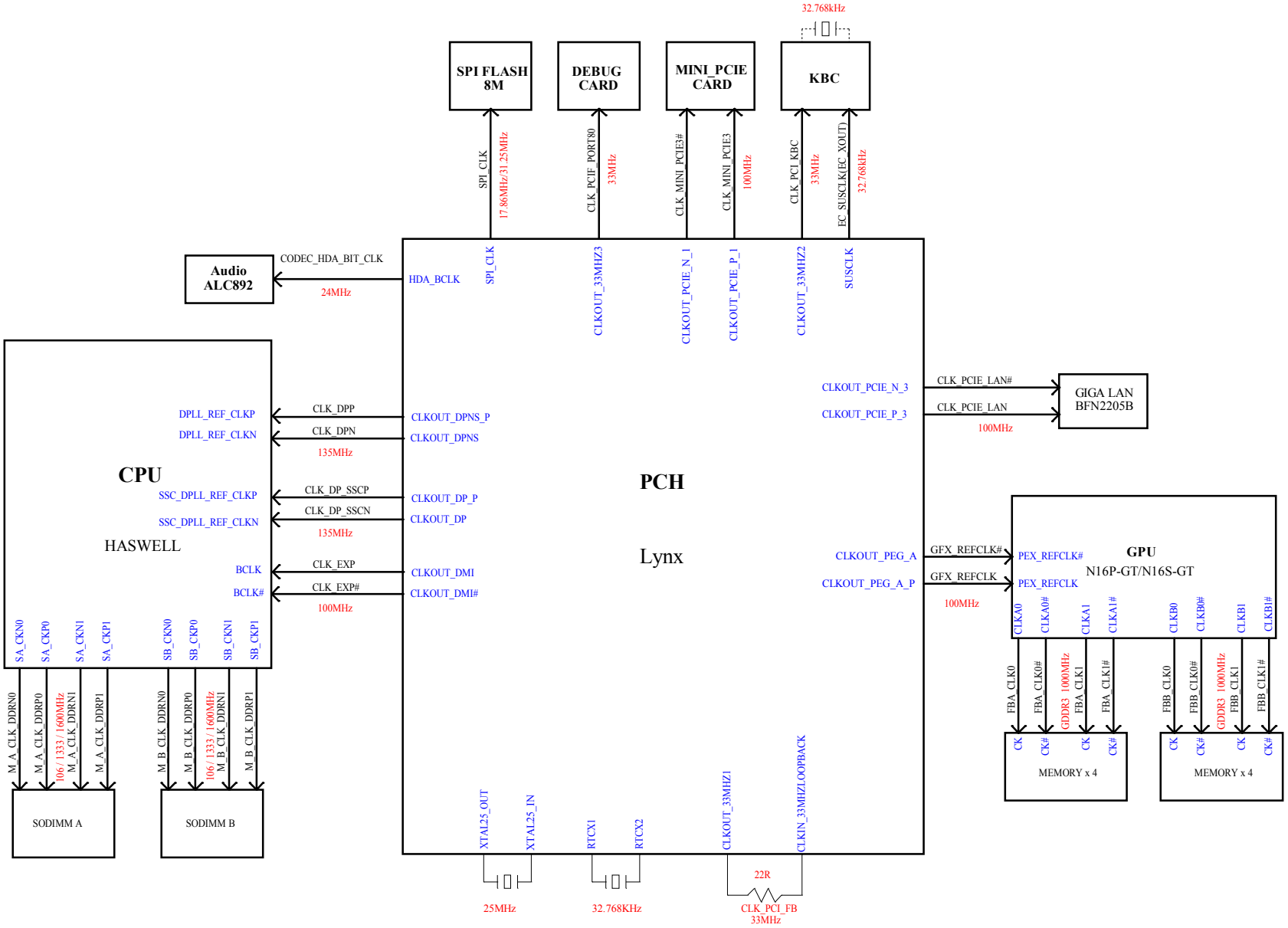

MICRO-STAR INT'L CO.,LTD.

Title: CLock Delivery chart

Size: Document Number: MS-16J3 Rev: 1.0

Date: Tuesday, April 14, 2015 Sheet 2 of 60

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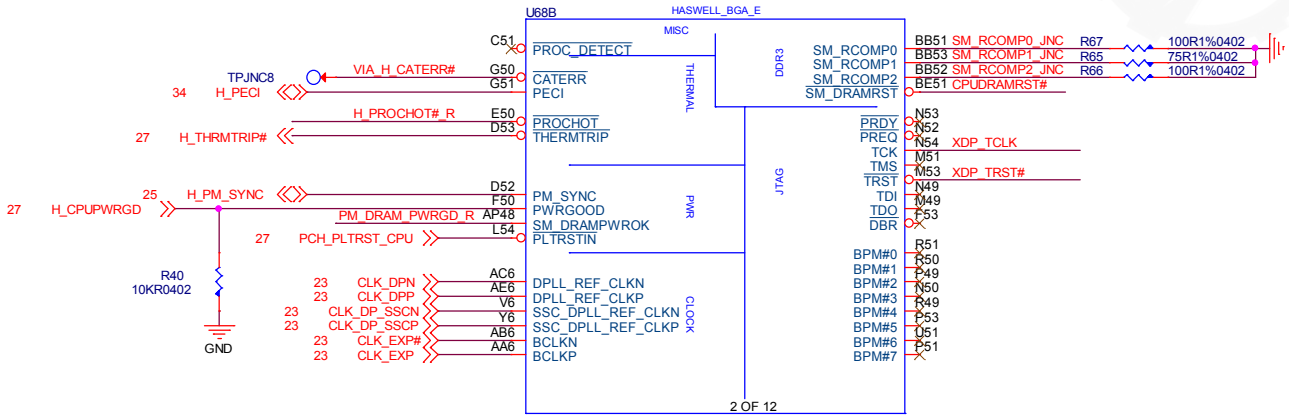
Haswell (DMI,PEG,FDI)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

Haswell (CLK,MISC,JTAG)

i7-4710HQ,(SR1PX),2.5GHz

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil



I7_4720

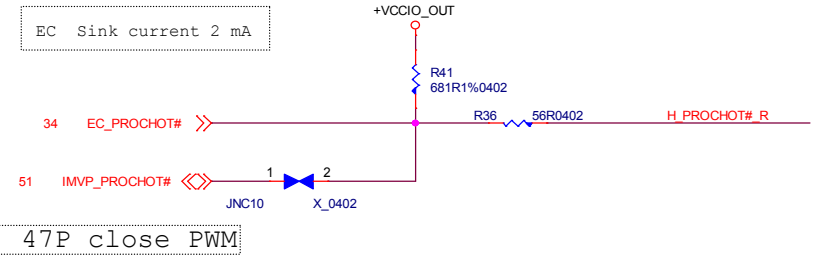
I7 4720 **HSW**

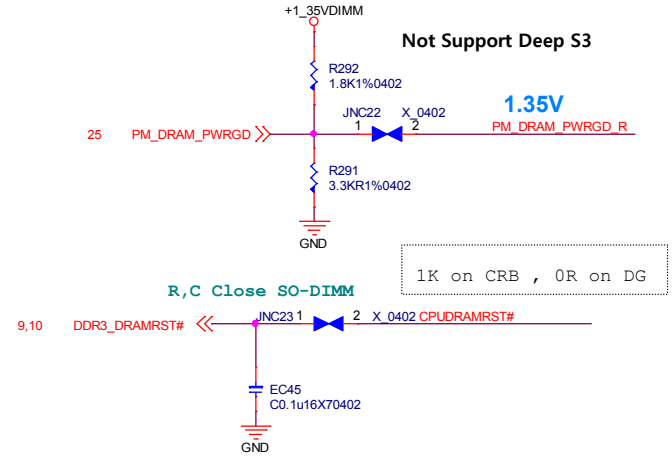
I7_4720
A13-2620135-I06

I7_5700

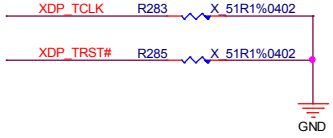
I7 5700 **BDW**

I7_5700
OAD-1812002





p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.



MICRO-STAR INT'L CO.,LTD.

Title	CPU-1 (Host Bus)	
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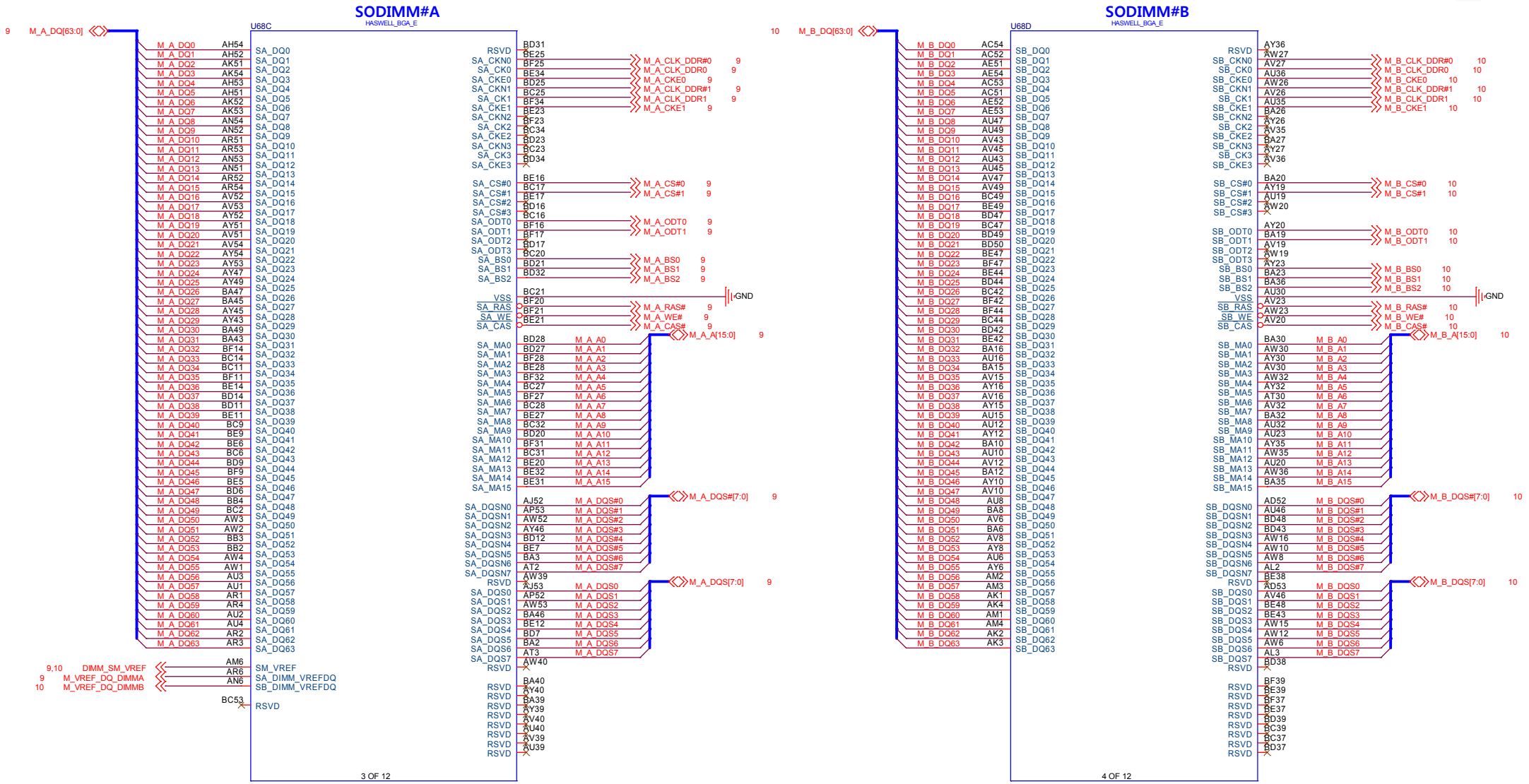
Haswell (DDR3L)



MICRO-STAR INT'L CO.,LTD.

Title	CPU-2 (DDR3L)	
Size	Document Number MS-16J3	Rev 1.0
Date: Tuesday, April 14, 2015	Sheet 4 of 60	

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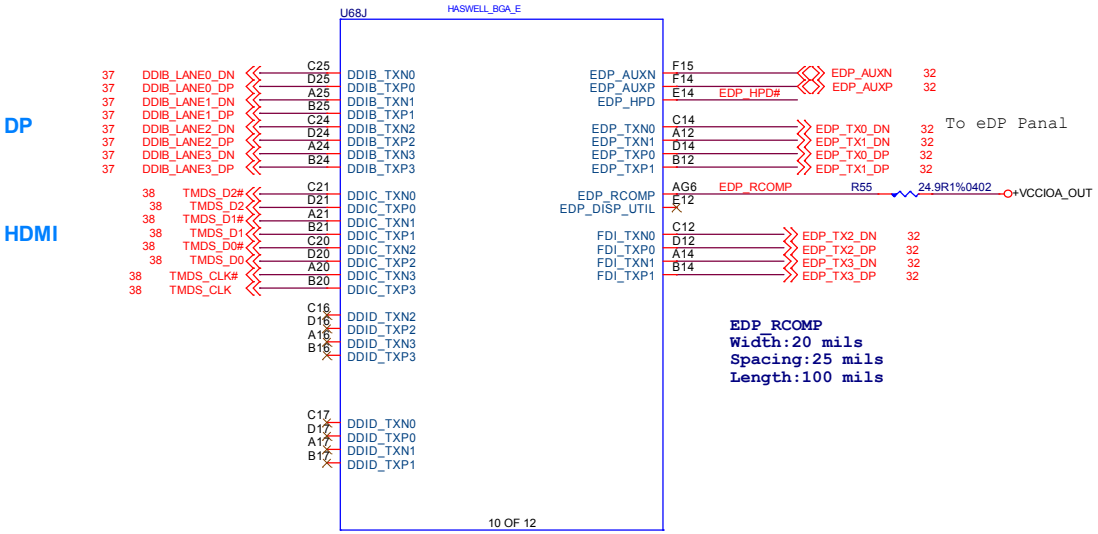
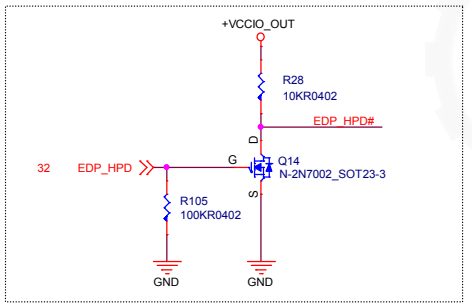
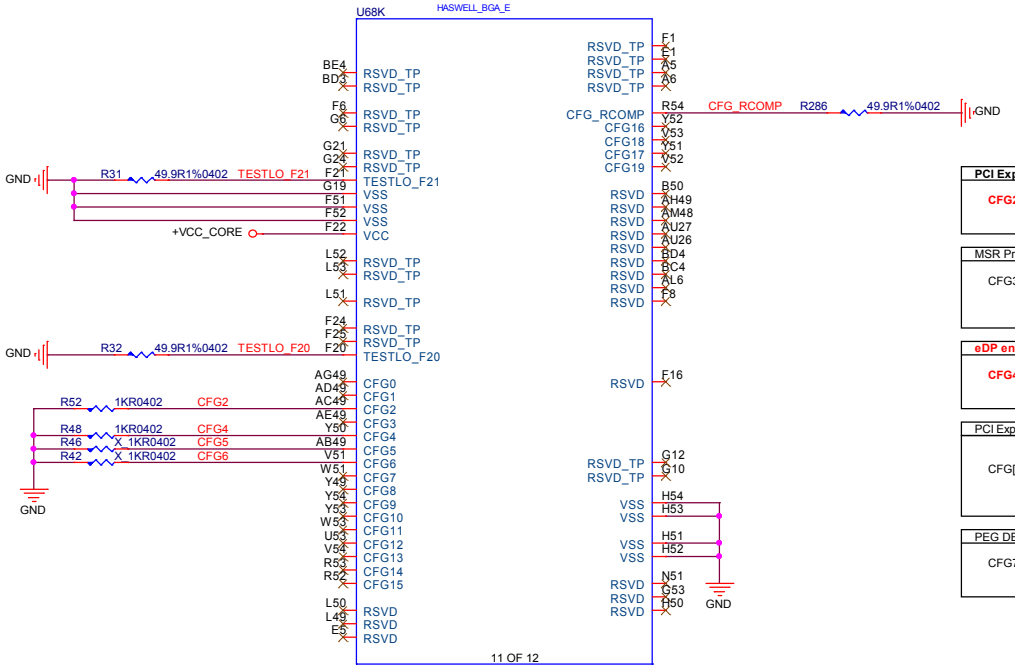
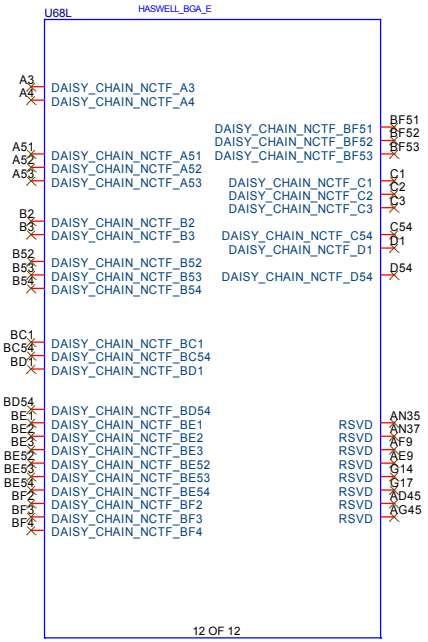
Display/Reserved



EDP_RCOMP
Width:20 mils
Spacing:25 mils
Length:100 mils







PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Title: CPU-3 (Display/Reserved)

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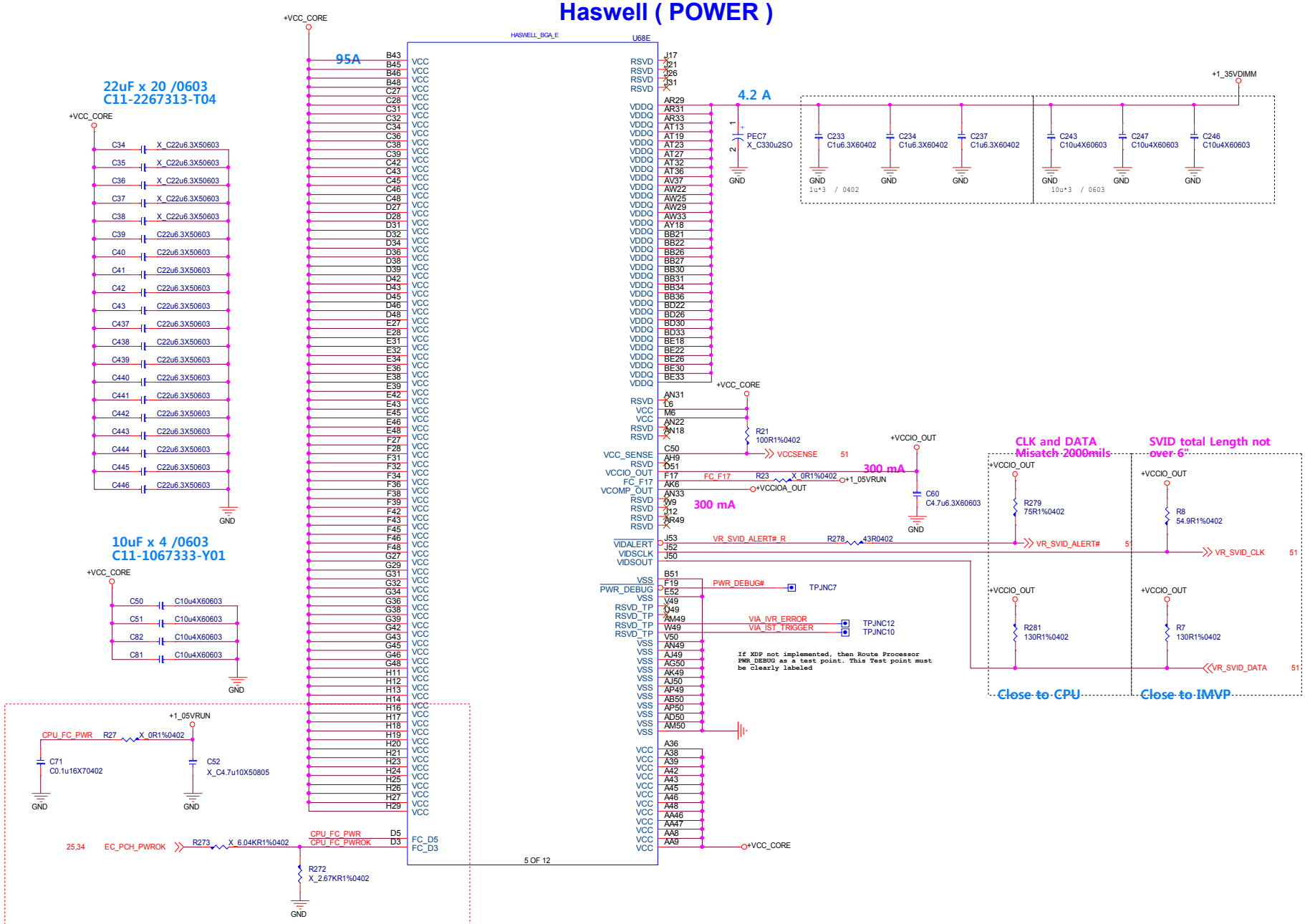
Haswell (POWER)



PIN D5&D3 Setting : 486713_Shark_Bay_Mobile_PDG

PIN D5&D3	
Haswell	NC
Broadwell	Stuff

MICRO-STAR INT'L CO.,LTD.	
Title	CPU-4 (Power)
Size	Document Number: MS-16J3
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Date:	Tuesday, April 14, 2015
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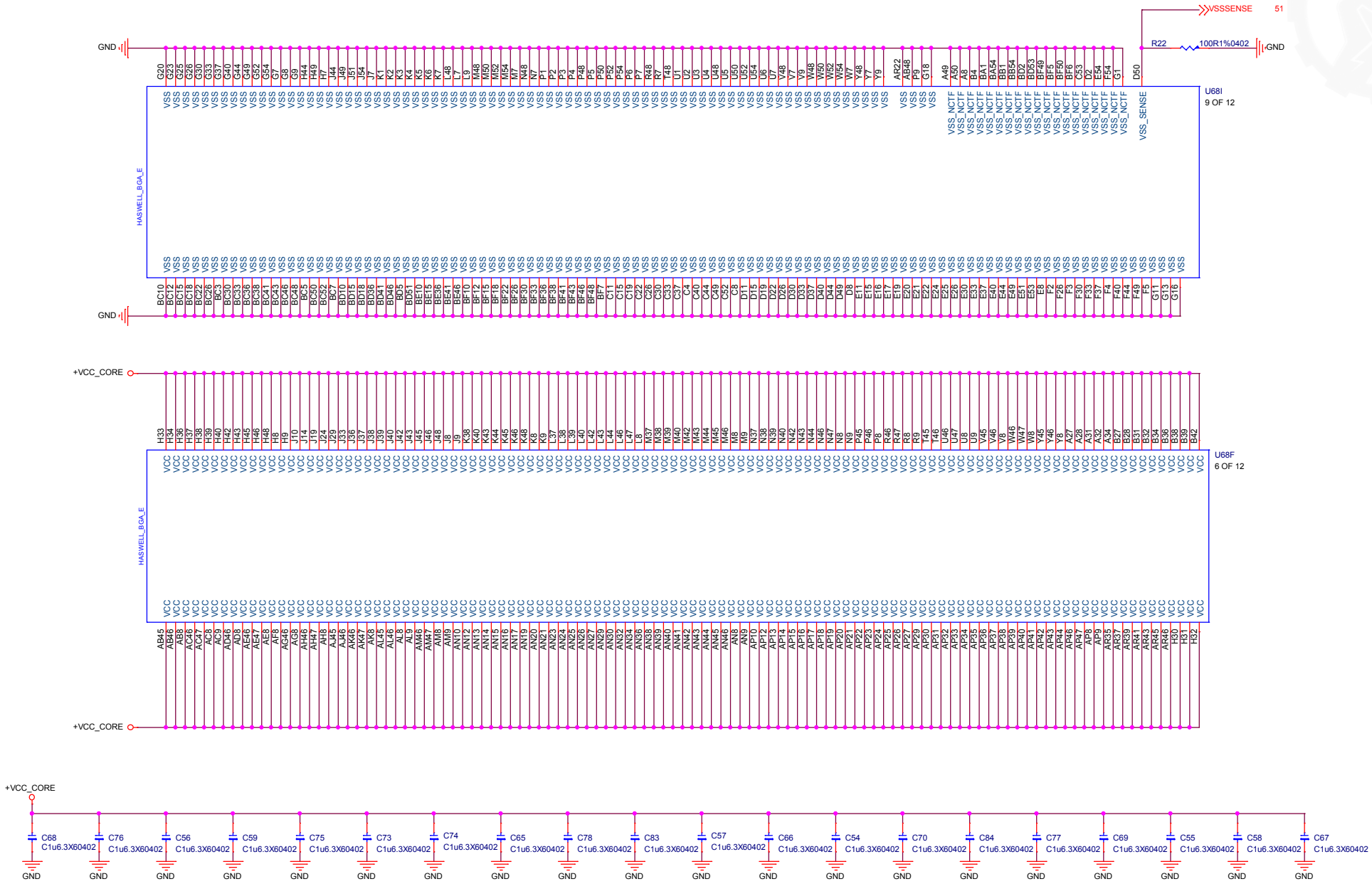
Haswell (Power & GND)



MICRO-STAR INT'L CO.,LTD.

Title	CPU-6 (Power & GND)	
Size	Document Number MS-16J3	Rev 1.0
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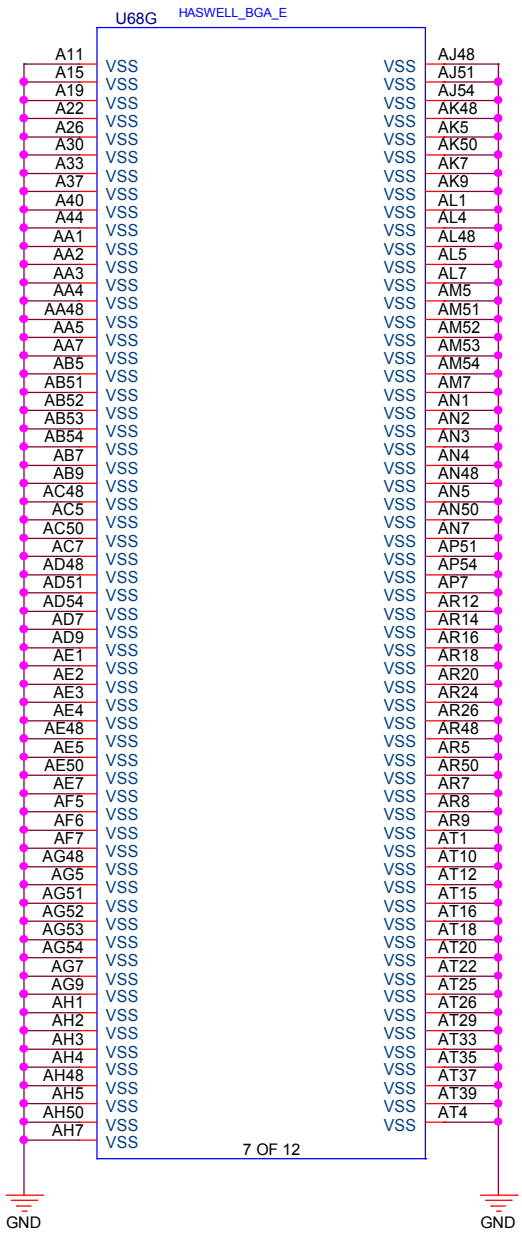
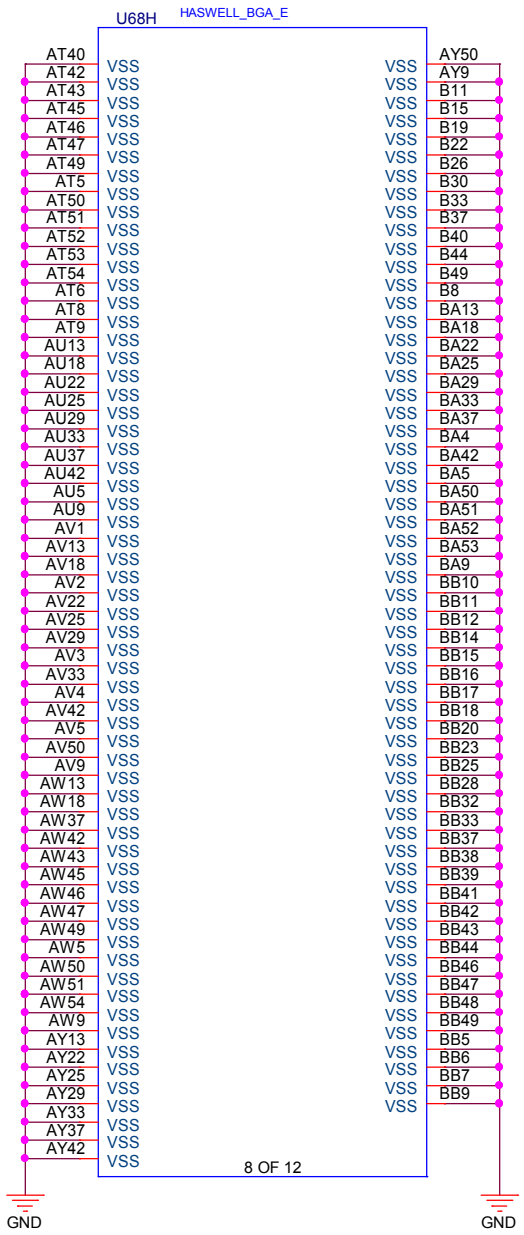
Haswell (GND)





MICRO-STAR INT'L CO.,LTD.		
Title: CPU-5 (GND)		
Size	Document Number: MS-16J3	Rev: 1.0
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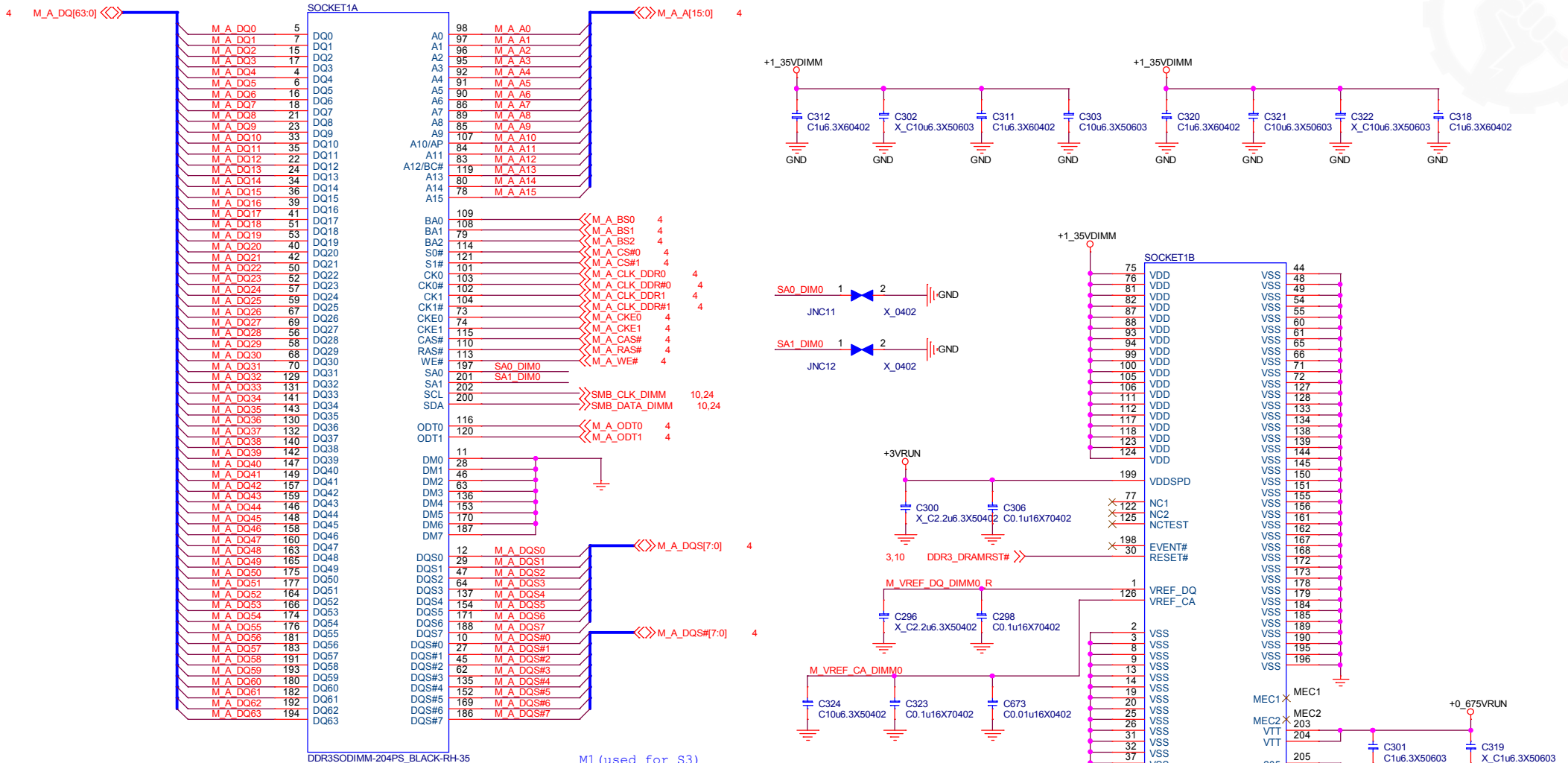
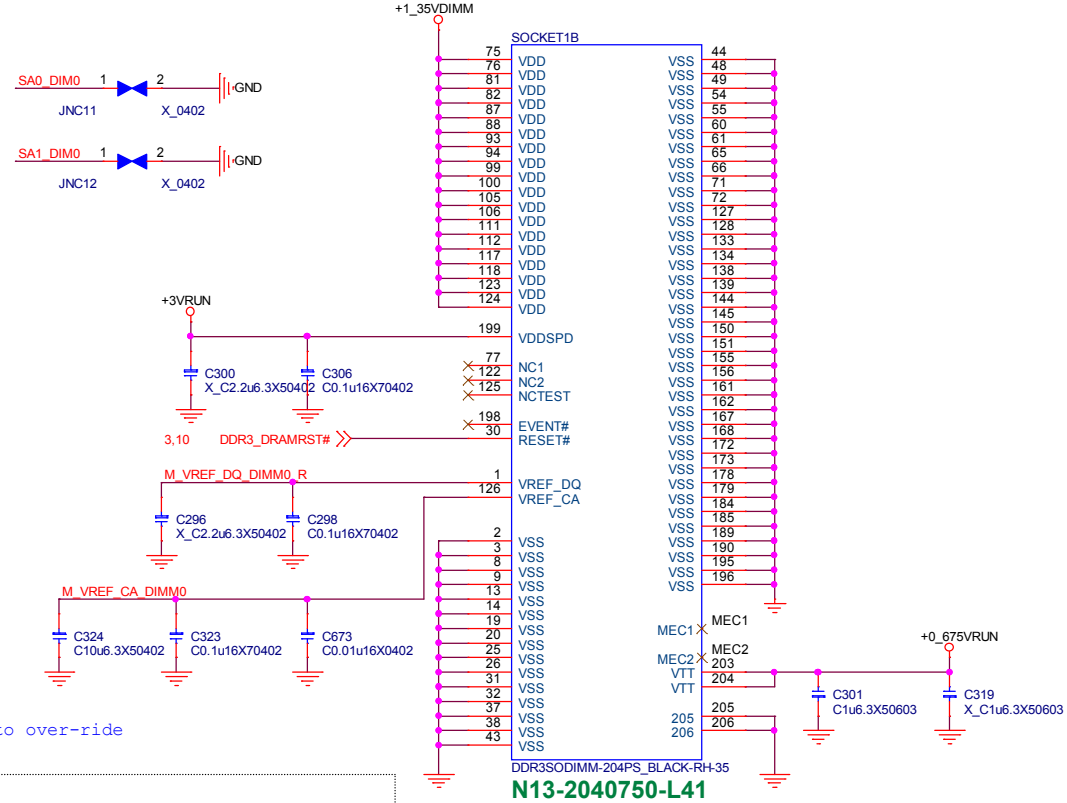
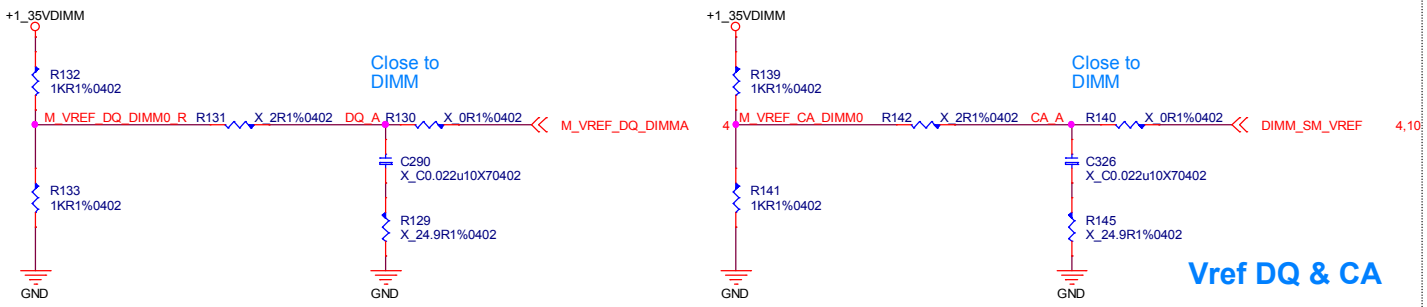
SODIMM#A



M1(used for S3)
M3(used for S0),maybe to over-ride
Active when soft-start





MICRO-STAR INT'L CO.,LTD.		
Title: DDR3L SODIMM 0		
Size	Document Number: MS-16J3	Rev: 1.0
Date: Tuesday, April 14, 2015	Sheet 9 of 60	

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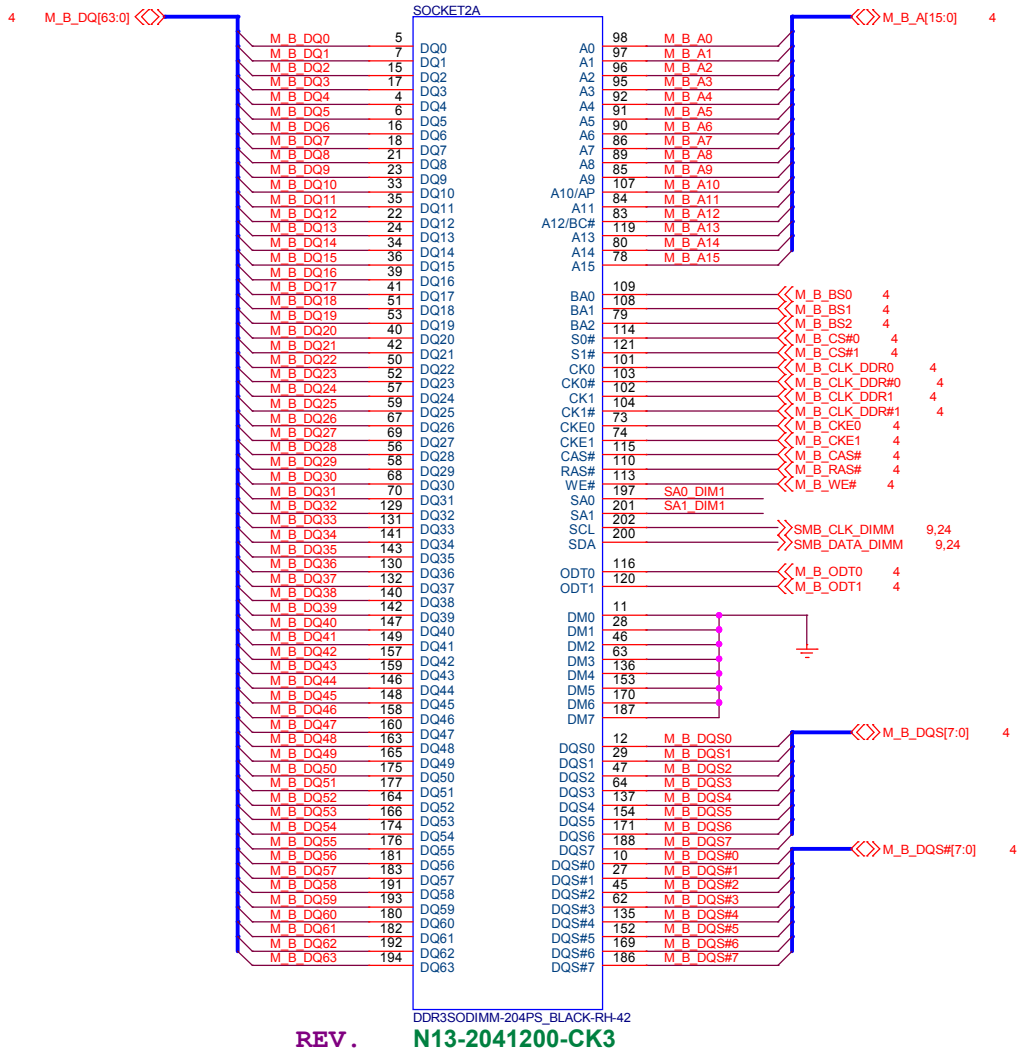
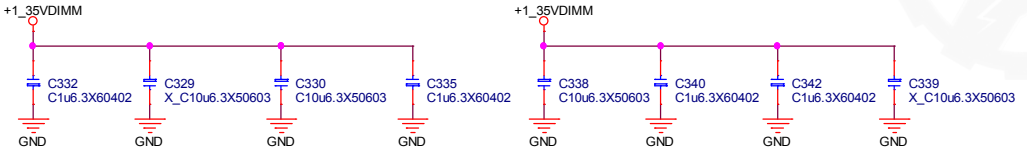
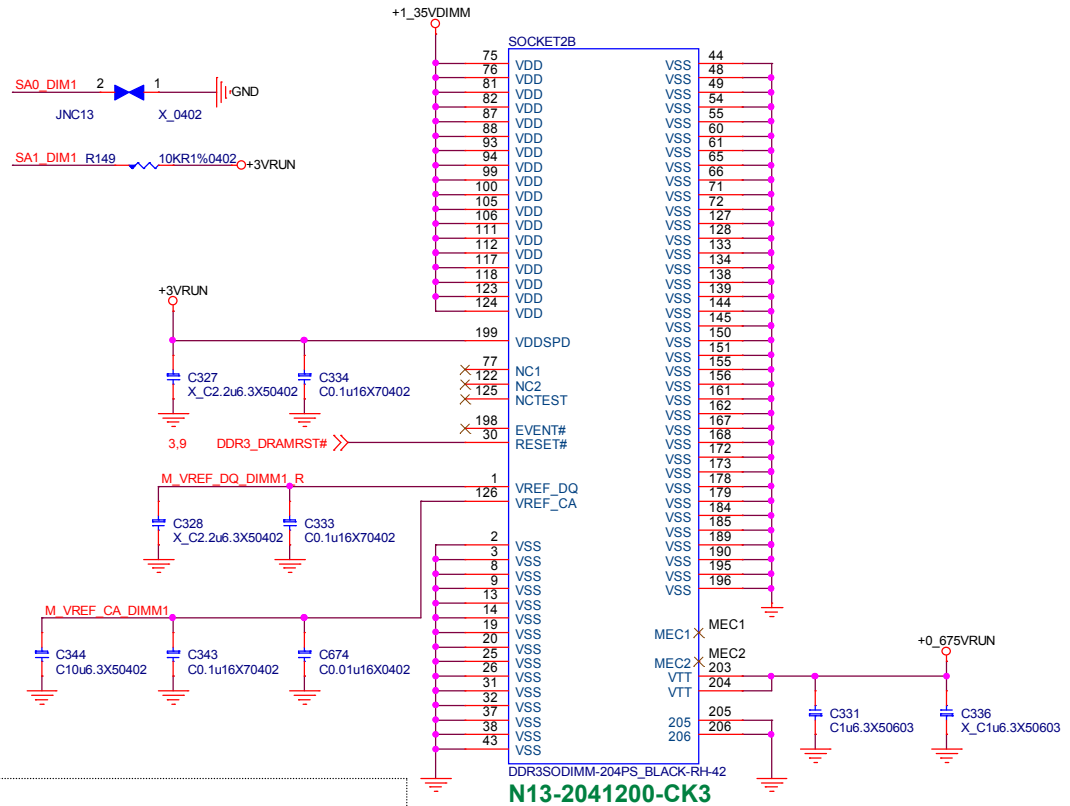
SODIMM#B

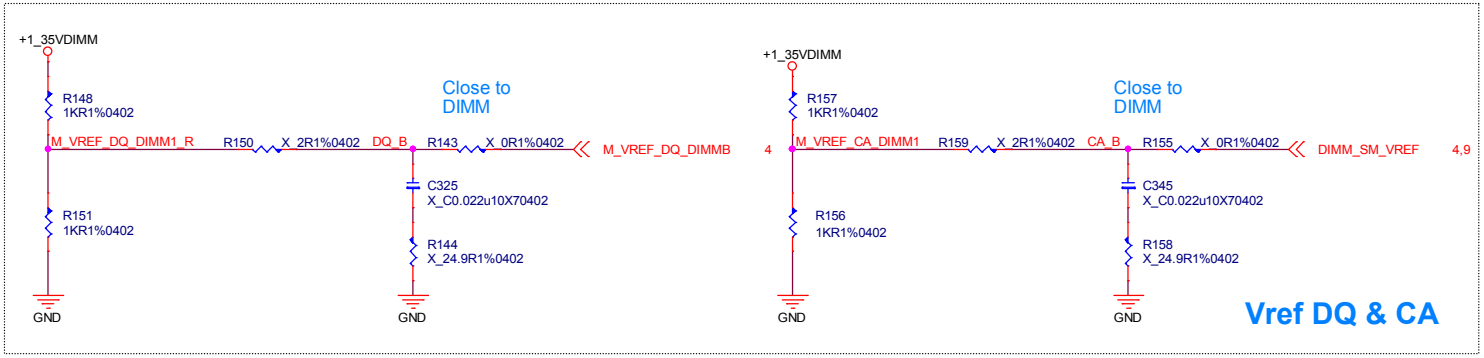


REV. N13-2041200-CK3





N13-2041200-CK3



MSI MICRO-STAR INT'L CO.,LTD.		
Title: DDR3L SODIMM 1		
Size	Document Number: MS-16J3	Rev: 1.0
Date: Tuesday, April 14, 2015	Sheet 10 of 60	

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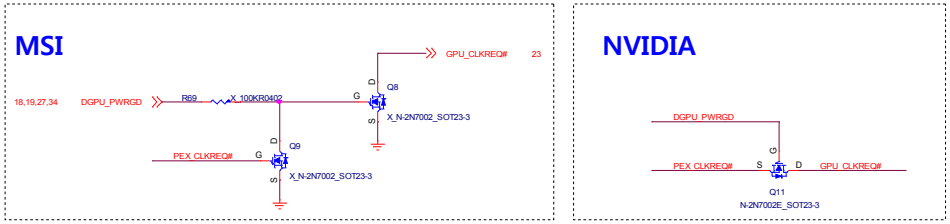
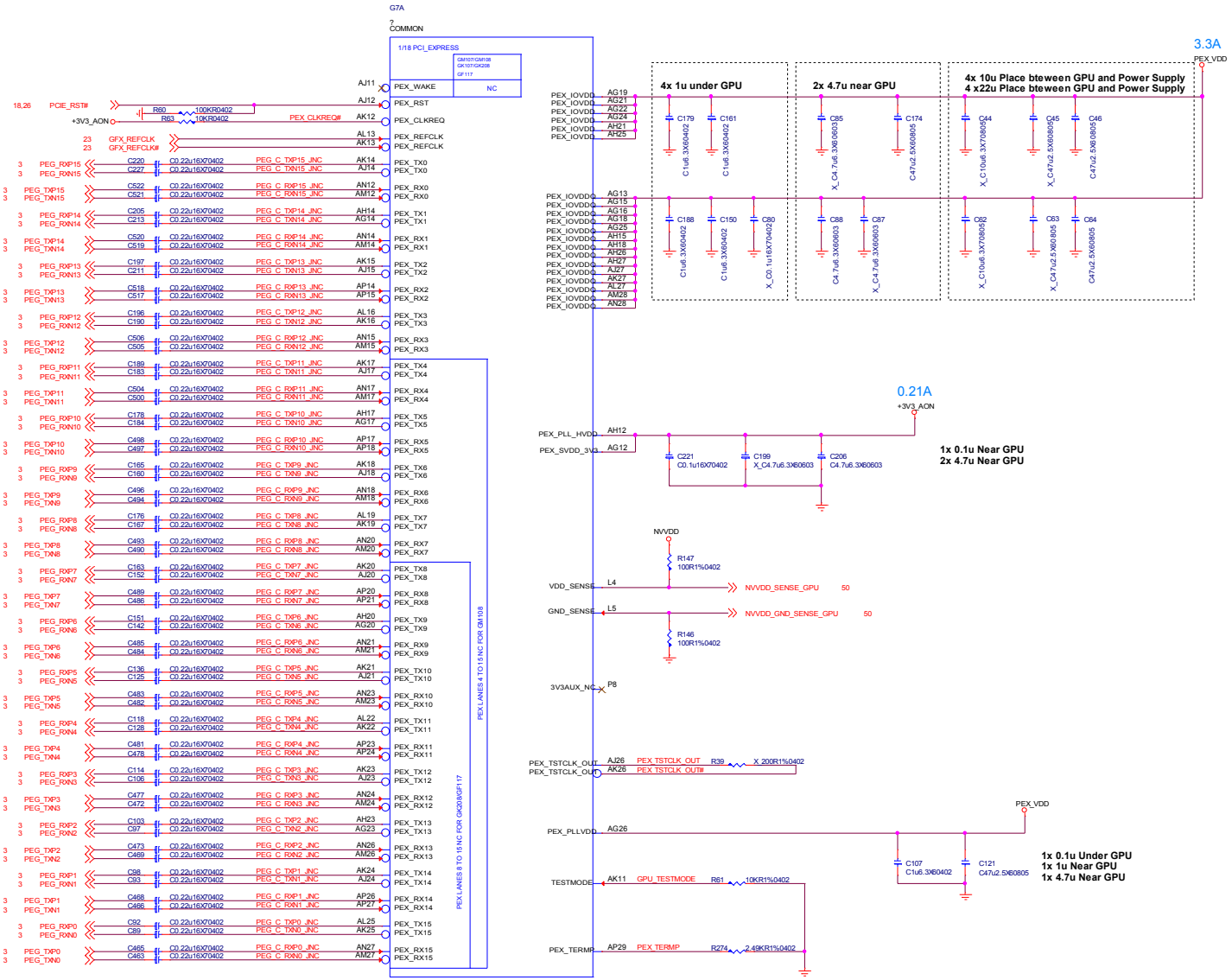
N16P-GT(PCI-Express Gen3 x16 Interface)





Title	N16P-GT_PCI-E Host		
Size	Custom	Rev	1.0
Date:	Thursday, March 14, 2015	Sheet	11 of 60

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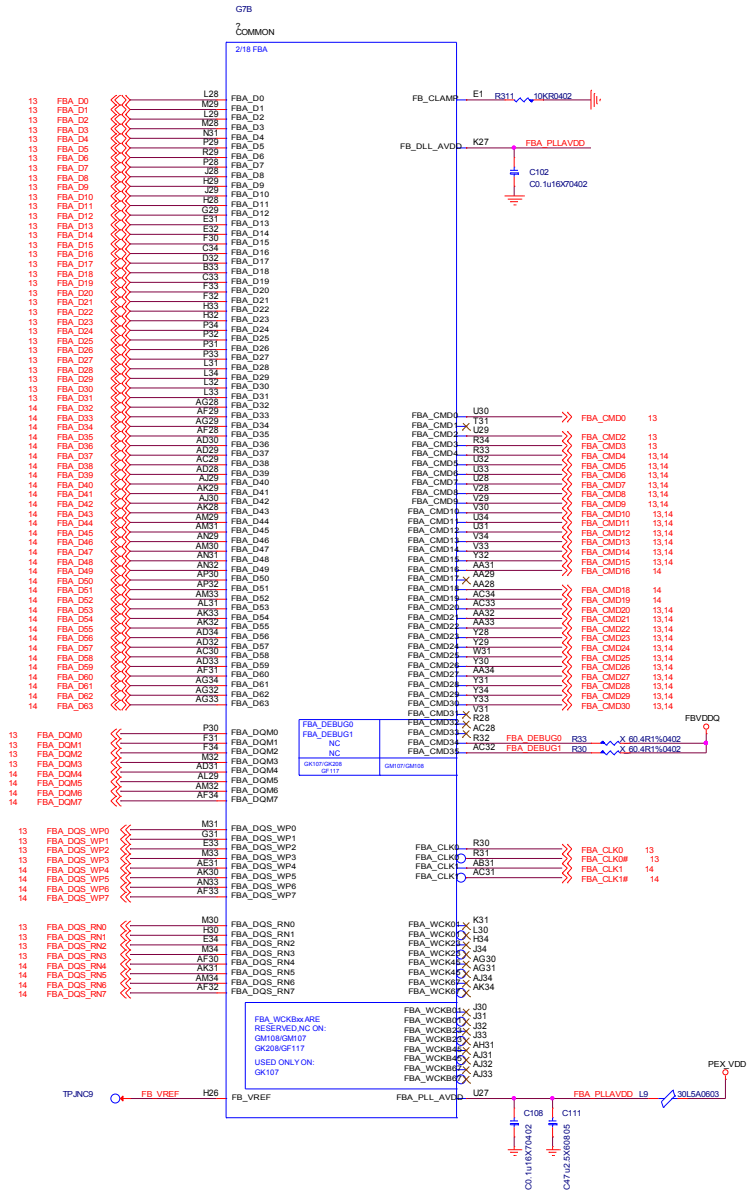
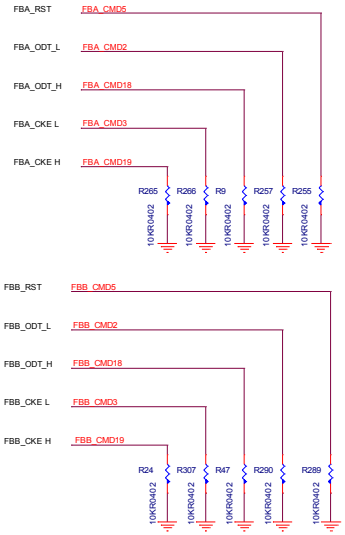
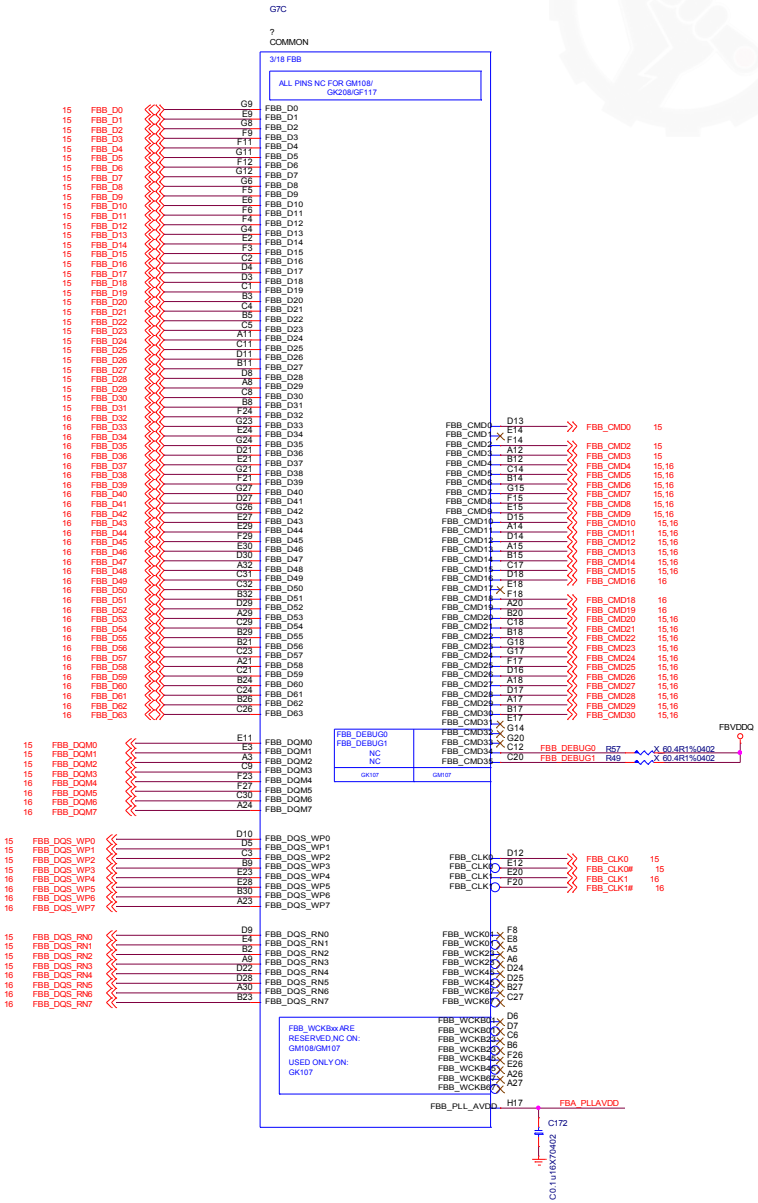
N16P-GT(Frame Buffer Interface)

	DATA[0:31]	DATA[32:63]
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD2	ODT	N/A
CMD3	CKE	N/A
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD18	N/A	ODT
CMD19	N/A	CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
CMD31	N/A	N/A
CMD32	N/A	N/A
CMD33	N/A	N/A
CMD34	DBG0	DBG0
CMD35	DBG1	DBG1







Title: N16P-GT_MEM IF A/B

Size: Custom | Document Number: MS-16J3 | Rev: 1.0

Date: Wednesday, May 14, 2015 | Sheet 12 of 60

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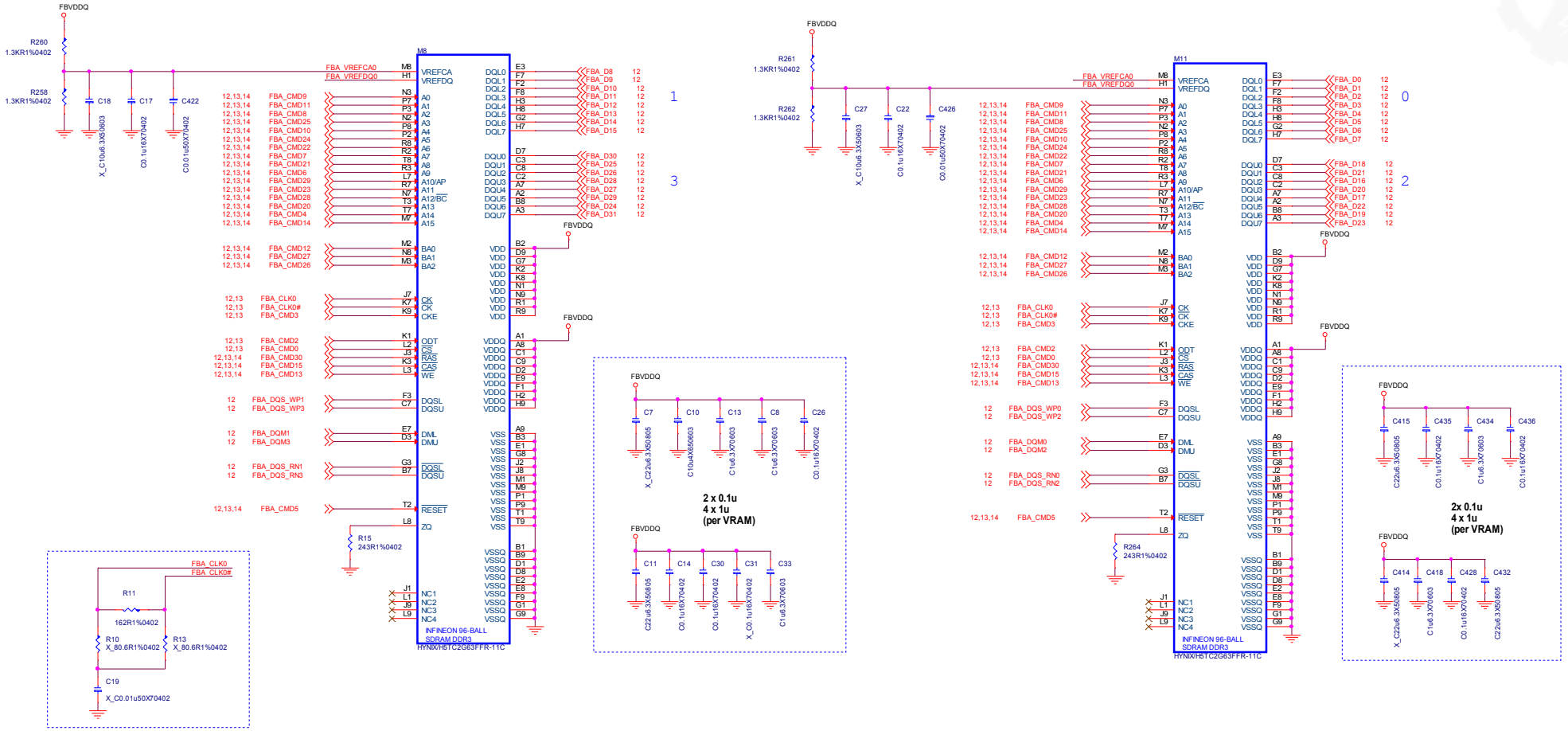
N16P-GT(GDDR3 Frame A-1)



Title	N16P-GT GDDR3 Frame A-1		
Size: Custom	Document Number: MS-1613		Rev: 1.0
Date: Wednesday, April 14, 2015	Sheet 13 of 60		

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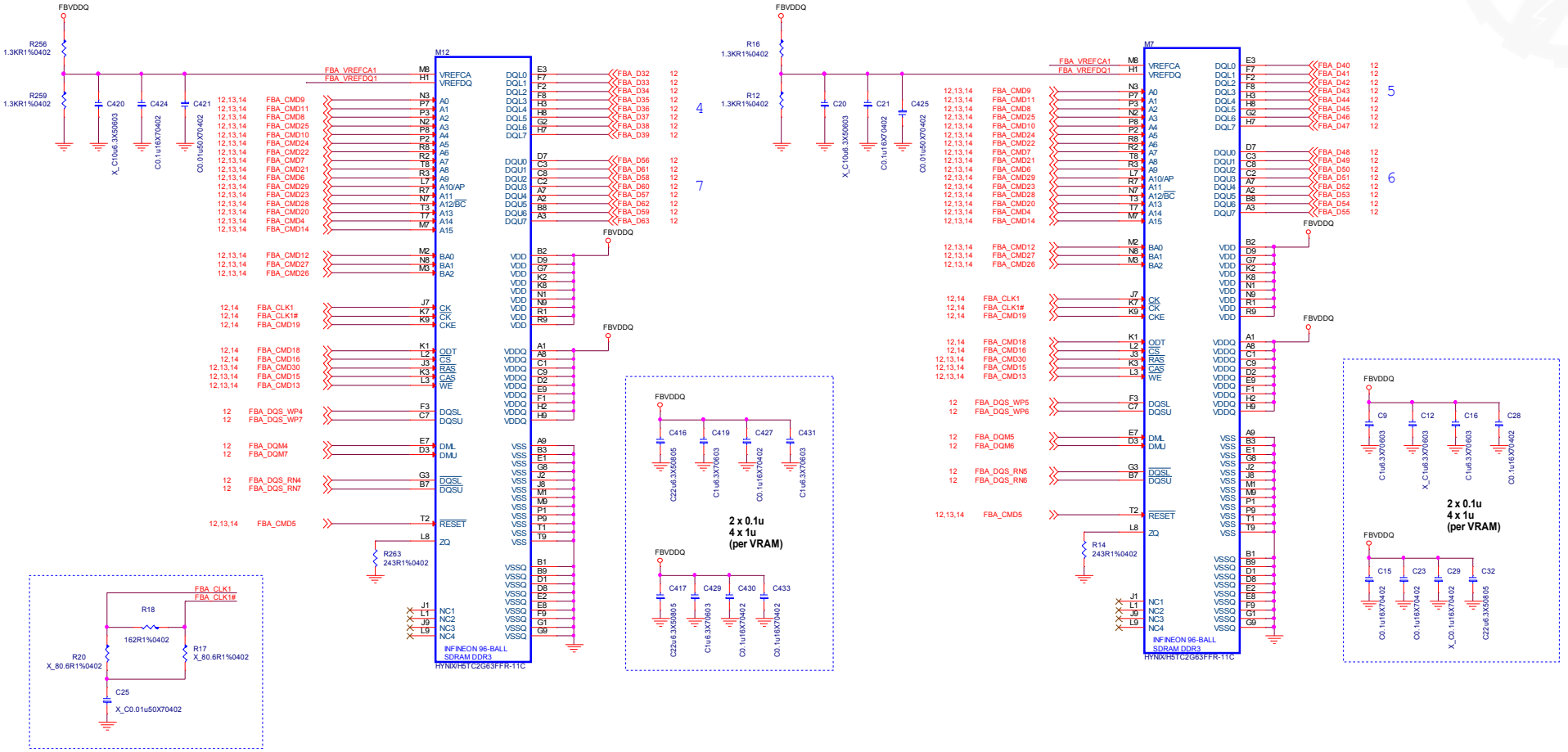
N16P-GT(GDDR3 Frame A-2)



Title	N16P-GT_GDDR3 Frame A-2		
Size	Document Number		Rev
Custom	MS-1613		1.0
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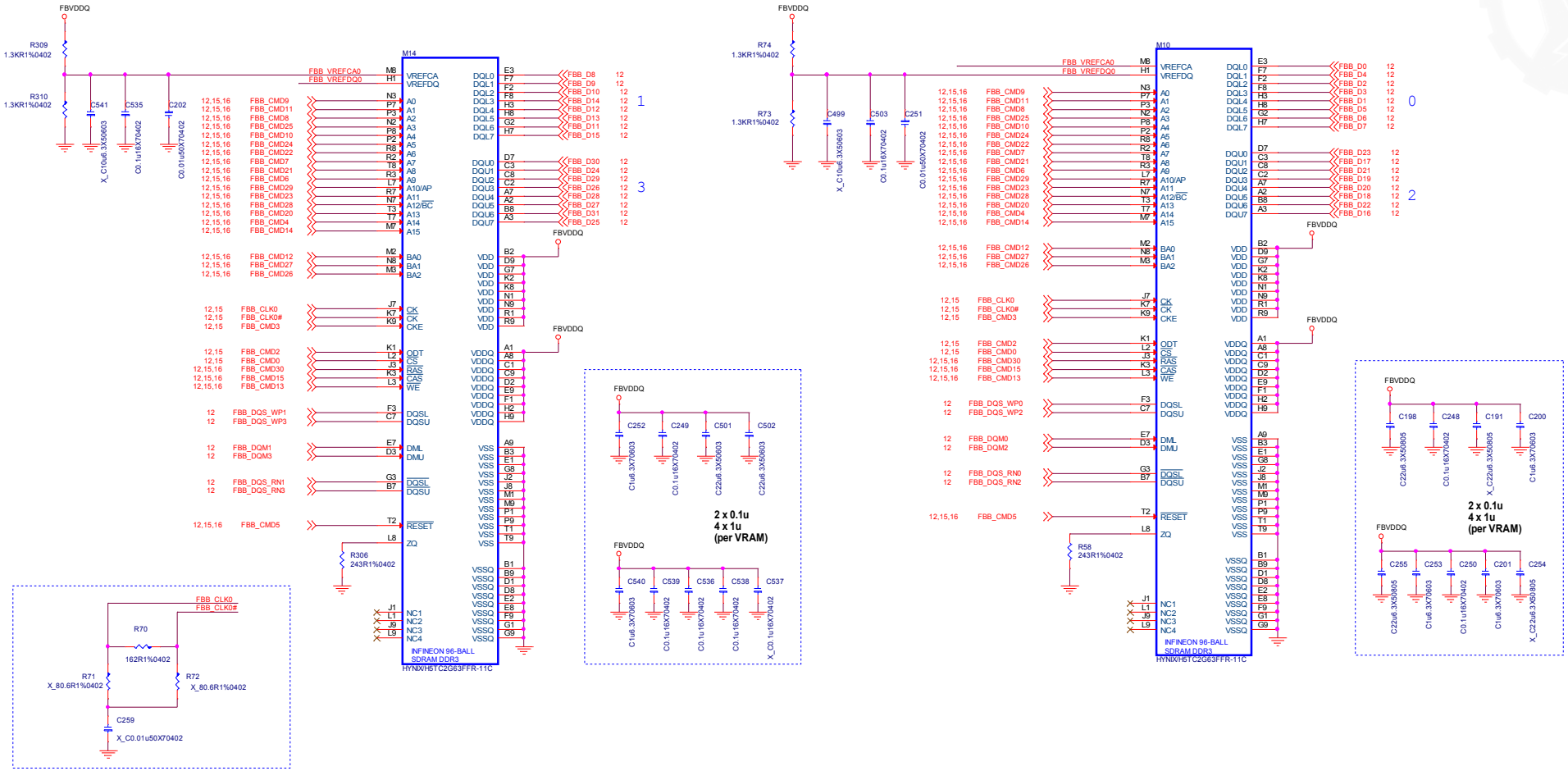
N16P-GT(GDDR3 Frame B-1)



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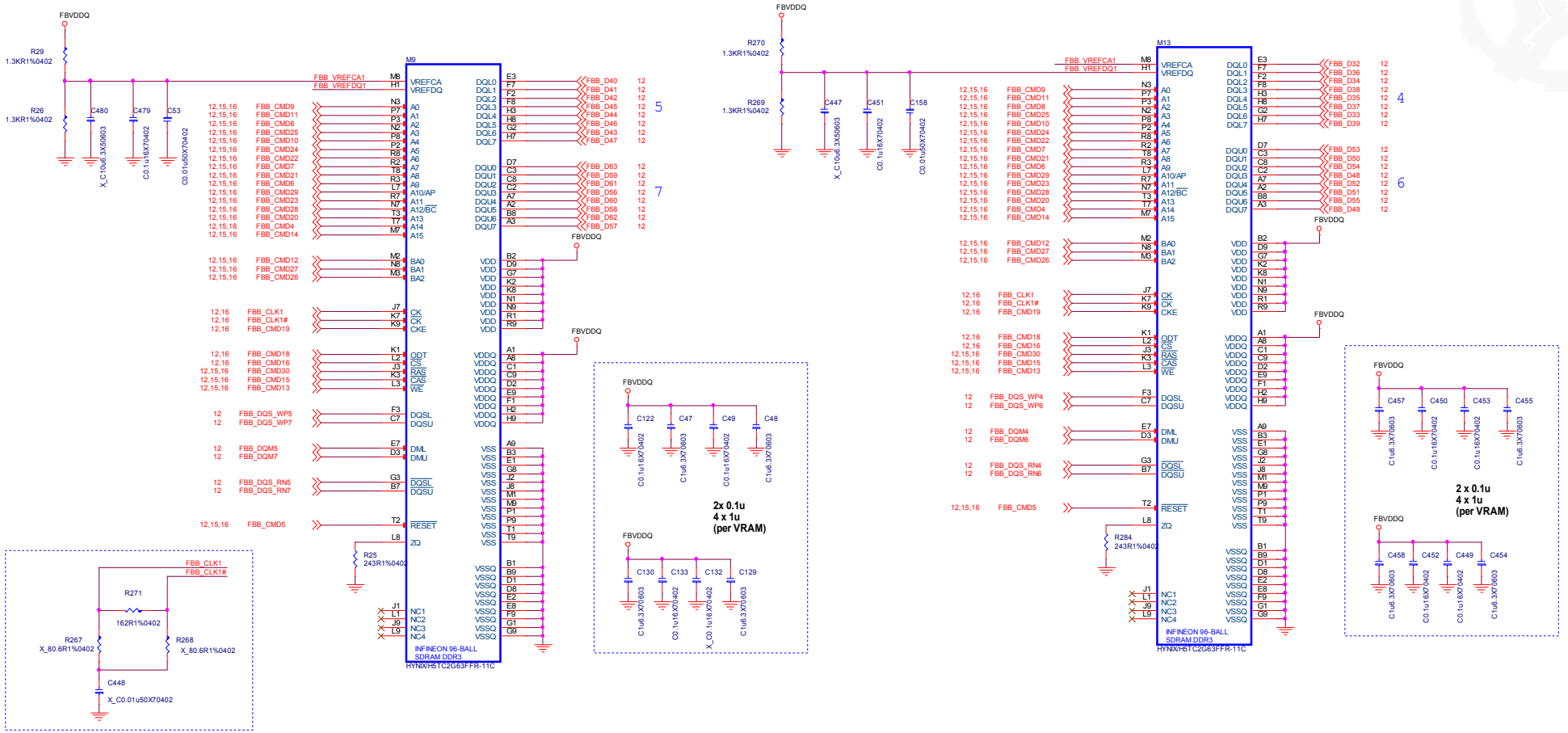
N16P-GT(GDDR3 Frame B-2)



Title	N16P-GT_GDDR3 Frame B-2	
Size: Custom	Document Number: MS-16J3	Rev: 1.0
Date: Wednesday, April 14, 2015	Sheet 16 of 60	

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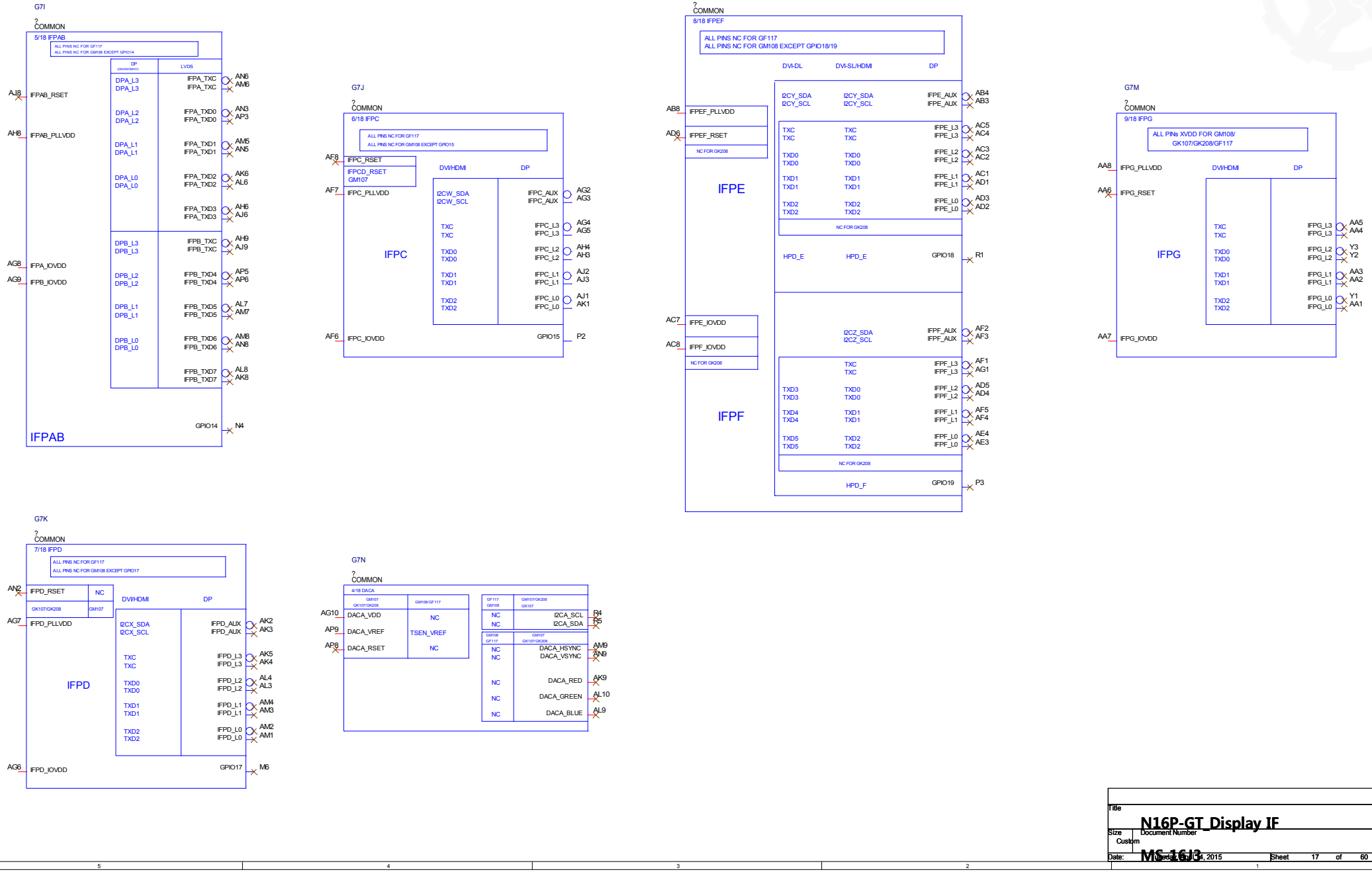
N16P-GT(Display IF)



Title	N16P-GT_Display IF		
Size	Document Number		Rev
Custom			1.0
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MS-16J3

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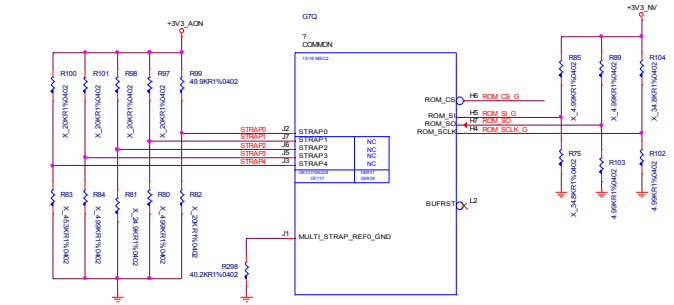
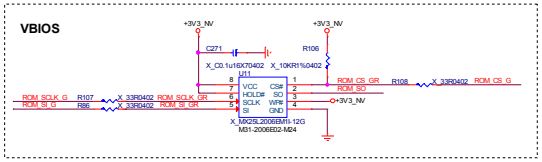
ROM / MULTI-LEVEL STRAPS / GPIO





N16P-GT

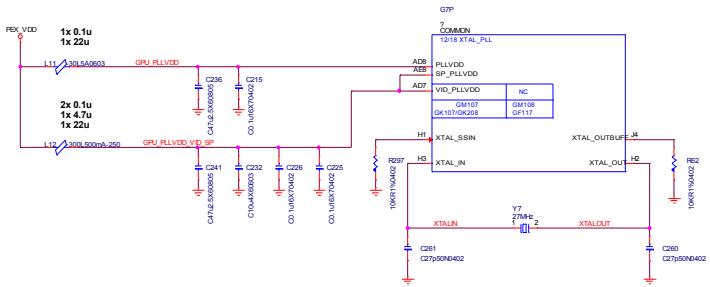
N16S-GT

N16P_GT_2G/N16S_GT_1G

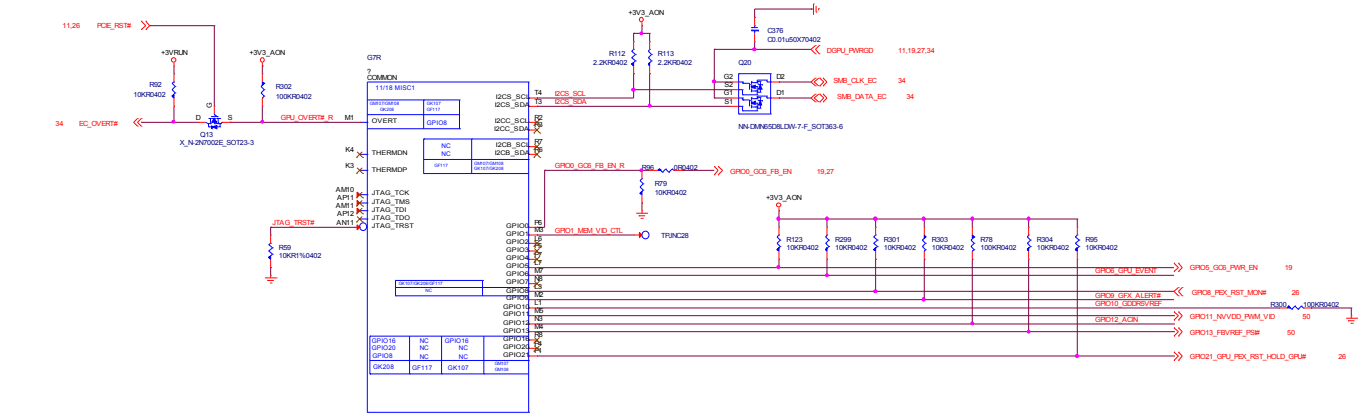
PD34K8	Hynix	V_TOP1		V_BOT1
	128Mx16bit		5010	5020
R11-3482T12-R01		M12-2G63F45-H23		M12-2G63F45-H23
X_34.8KR1%0402		X_H5TC2G63FFR-11C		X_H5TC2G63FFR-11C
PU4K9	Samsung	V_TOP2		V_BOT2
	128Mx16bit		5010	5020
R11-4991T12-W08		M12-K4W2GH5-S02		M12-K4W2GH5-S02
X_4.99KR1%0402		X_K4W2G1646Q-BC1A		X_K4W2G1646Q-BC1A

N16P_GT_4G/N16S_GT_2G

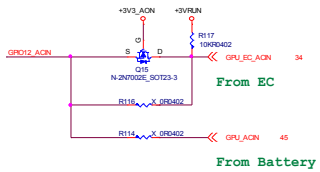
PD30K1	Hynix	V_TOP3		V_BOT3
	256Mx16bit		5010	5020
R11-3012T12-W08		M12-4G63C35-H23		M12-4G63C35-H23
X_30.1KR1%0402		X_H5TC4G63CFR-N0C		X_H5TC4G63CFR-N0C
PD15K	Samsung	V_TOP4		V_BOT4
	256Mx16bit		5010	5020
R11-0153T12-W08		M12-1646D25-S02		M12-1646D25-S02
X_15KR1%0402		X_K4W4G1646D-BC1A		X_K4W4G1646D-BC1A

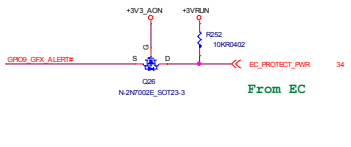


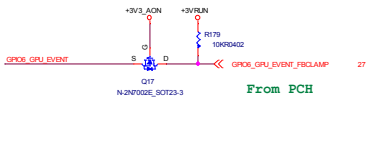
Item	Location	N16P-GT	N16S-GT	N16S-GM
Device ID		0x139A	0x1347	0x1346
Package		GB4B-128	GB4B-128	GB4B-128
Memory Type		DDR3	DDR3	DDR3
Device Specific Strap Mode Selection	R298	Multi_Strap_Ref0_GND,40.2K PD to GND	Multi_Strap_Ref0_GND,40.2K PD to GND	Multi_Strap_Ref0_GND,40.2K PD to GND
ROM_SI	R85 R75	0x6, Hynix 2G, 34.8kohm pull down 0x8, Samsung 2G, 4.99Kohm pull up 0x9, Hynix 4G, 30.1kohm pull down 0x2, Samsung 4G, 15Kohm pull down	0x6, Hynix 2G, 34.8kohm pull down 0x8, Samsung 2G, 4.99Kohm pull up 0x9, Hynix 4G, 30.1kohm pull down 0x2, Samsung 4G, 15Kohm pull down	0x6, Hynix 2G, 34.8kohm pull down 0x8, Samsung 2G, 4.99Kohm pull up 0x9, Hynix 4G, 30.1kohm pull down 0x2, Samsung 4G, 15Kohm pull down
ROM_SO	R103	4.99Kohm pull down	4.99Kohm pull down	4.99Kohm pull down
ROM_SCLK	R102	4.99Kohm pull down	4.99Kohm pull down	4.99Kohm pull down
Strap0	R99	49.9Kohm pull up	49.9Kohm pull up	49.9Kohm pull up
Strap1		NC	NC	NC
Strap2		NC	NC	NC
Strap3		NC	NC	NC
Strap4		NC	NC	NC



Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GC6_FB_EN(GPIO0_GC6_FB_EN)	O	FB Enable for GC6 2.0	10K pull-down
GPIO1	MEM_VDD_CTL(NC)	O	Memory VDD VID	
GPIO2	LCD_BL_PWM(NC)	O	Panel Backlight PWM Brighteness Control	
GPIO3	LCD_VCC(NC)	O	Panel Power Enable	
GPIO4	LCD_BLEN(NC)	O	Panel Backlight Enable	
GPIO5	3V3_MAIN_EN(GPIO5_GC6_PWR_EN)	O	GPU POWER Sequencing	10K pull-up to 3V3 _AON
GPIO6	GPU_EVENT#(GPIO6_GPU_EVENT_FBCLAMP)	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3 _AON
GPIO7	3DVision(NC)	O	3D Vision L/R signal	
GPIO8	SYS_PEX_RST_MON#(GPIO8_PEX_RST_MON#)	I	System side PCI reset Monitor	10K pull-up to 3V3 _AON
GPIO9	ALERT(EC_PROTECT_PWR)	I/O	Active Low Thermal Alert	10K pull-up to 3V3 _AON
GPIO10	MEM_VREF_CTL(GPIO10_GDDR5VREF)	O	Memory VREF Control	100K pull-down
GPIO11	PWR_VID(GPIO11_GPUVID)	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL(GPIO12_ACIN)	I	AC power detect or power supply overdraw input	100K pull-up to 3V3 _AON
GPIO13	PSI(GPIO13_FBVREF_PSI#)	O	Phase shedding	10K pull-up to 3V3 _AON
GPIO14	HPD_A(NC)	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	
GPIO15	HPD_C(NC)	I	Hot Plug Detect for IFPC	
GPIO16	FRAME_LOCK#(NC)	I	Active Low Frame Lock	
GPIO17	HPD_D(NC)	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E(NC)	I	Hot Plug Detect for IFPE	
GPIO19	HPD_F or HPD_B(NC)	I	Hot Plug Detect for IFPF or for IFPFB when used as DisplayPort	
GPIO20	RESERVED			
GPIO21	GPU_PEX_RST_HOLD (GPIO21_GPU_PEX_RST_HOLD_GPU#)	O	GPU PCIE self-reset control	10K pull-up to 3V3 _AON
OVERT	OVERT(OVERT#)	O	Active Low Thermal Catastrophic Over Temperature	100K pull-up to 3V3 _AON







Title: N16P-GT_ROM & Straps & GPIO
Size: Custom | Document Number: MS-1813 | Rev: 1.0
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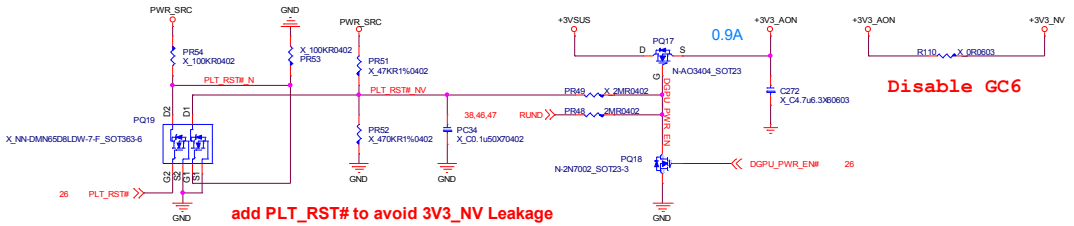
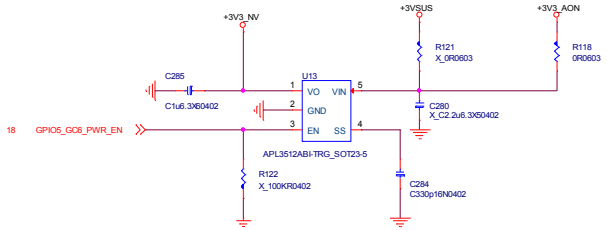
N16P-GT(Power Control)

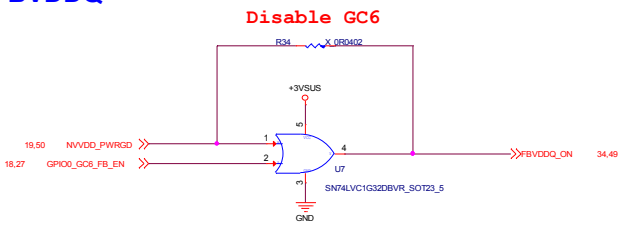
+3V3_AON -> +3V3_NV -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD

3.3V

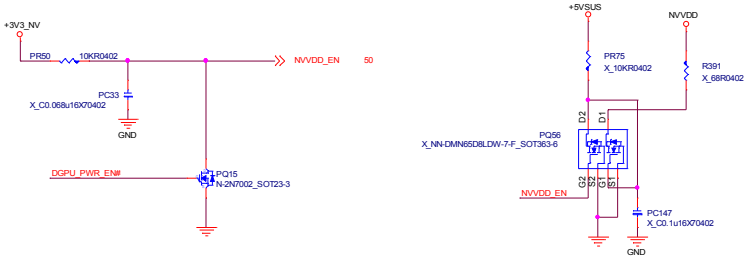




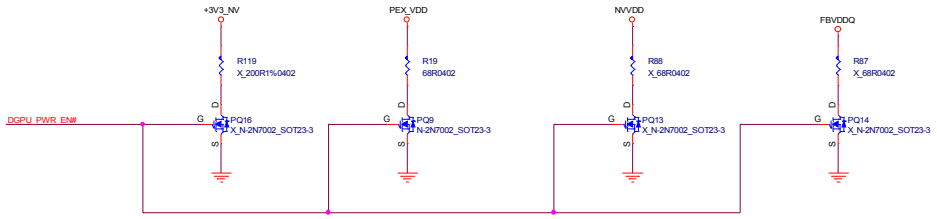
FBVDDQ



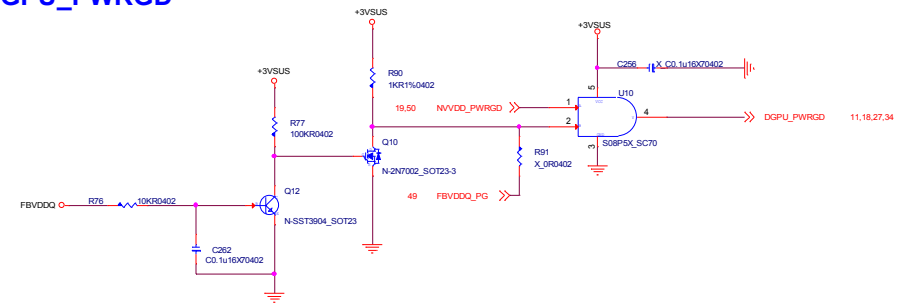
NVVDD



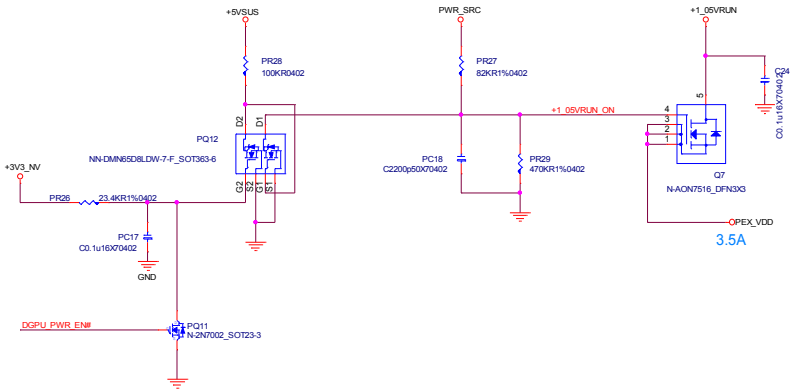
Discharge Circuit



DGPU_PWRGD



PEX_VDD



Title	N16P-GT Power Control	
Size: Custom	Document Number: ""	Rev: 1.0
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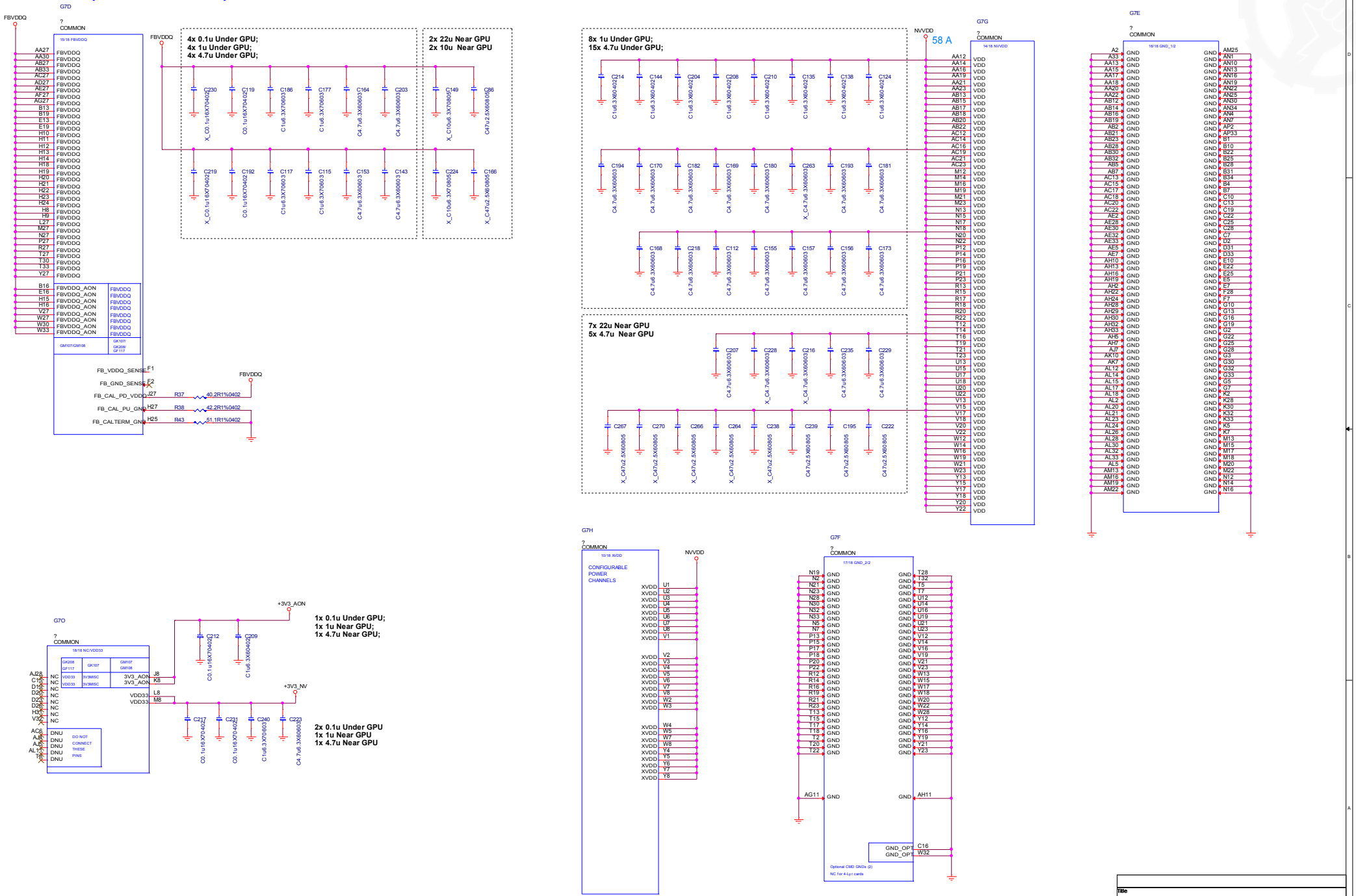
N16P-GT(Power & GND)



Title: N16P-GT Power & GND

Size: Custom | Document Number | Rev: 1.0

Date: Monday, May 04, 2015 | Sheet 20 of 60

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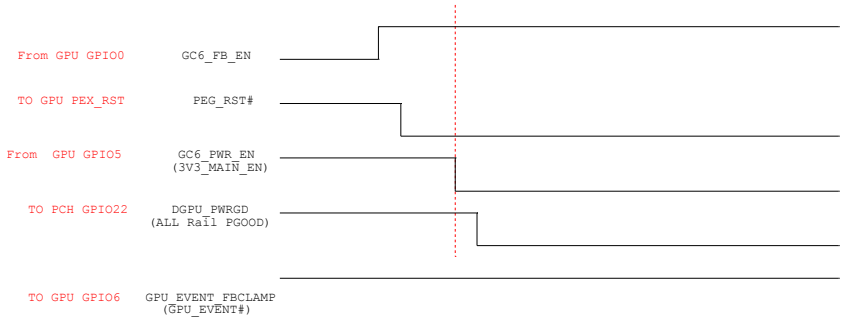
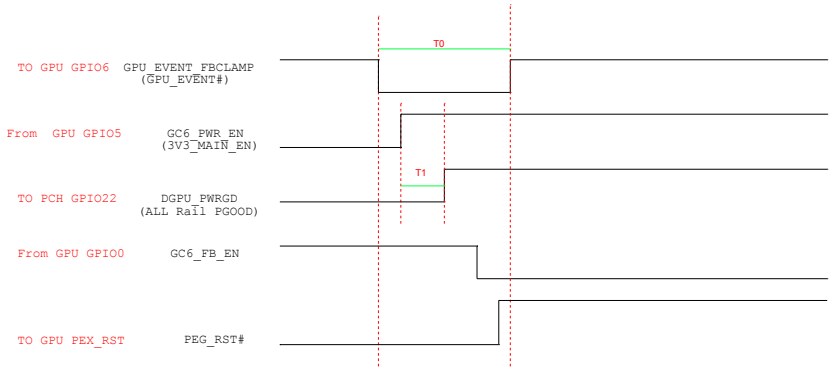
GC6 2.0 ENTRY SEQUENCE



GC6 2.0 EXIT SEQUENCE



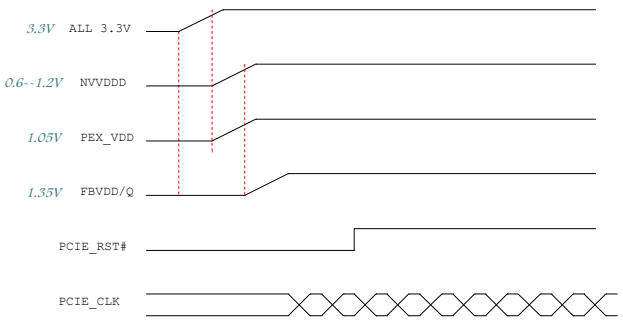
GC6 2.0 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	mS	GPU_EVENT# assertion
T1	0.04	4	mS	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation.
   If any GPU power rail cannot ge guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

GPU POWER ON SEQUENCE



NOTES:

1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltagr.
3. A VDD33 must ramp up to 90% before NVVDD and PEX_VDD in sequence can ramping up.
   NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

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Title: DGPU_POWER SEQUENCE

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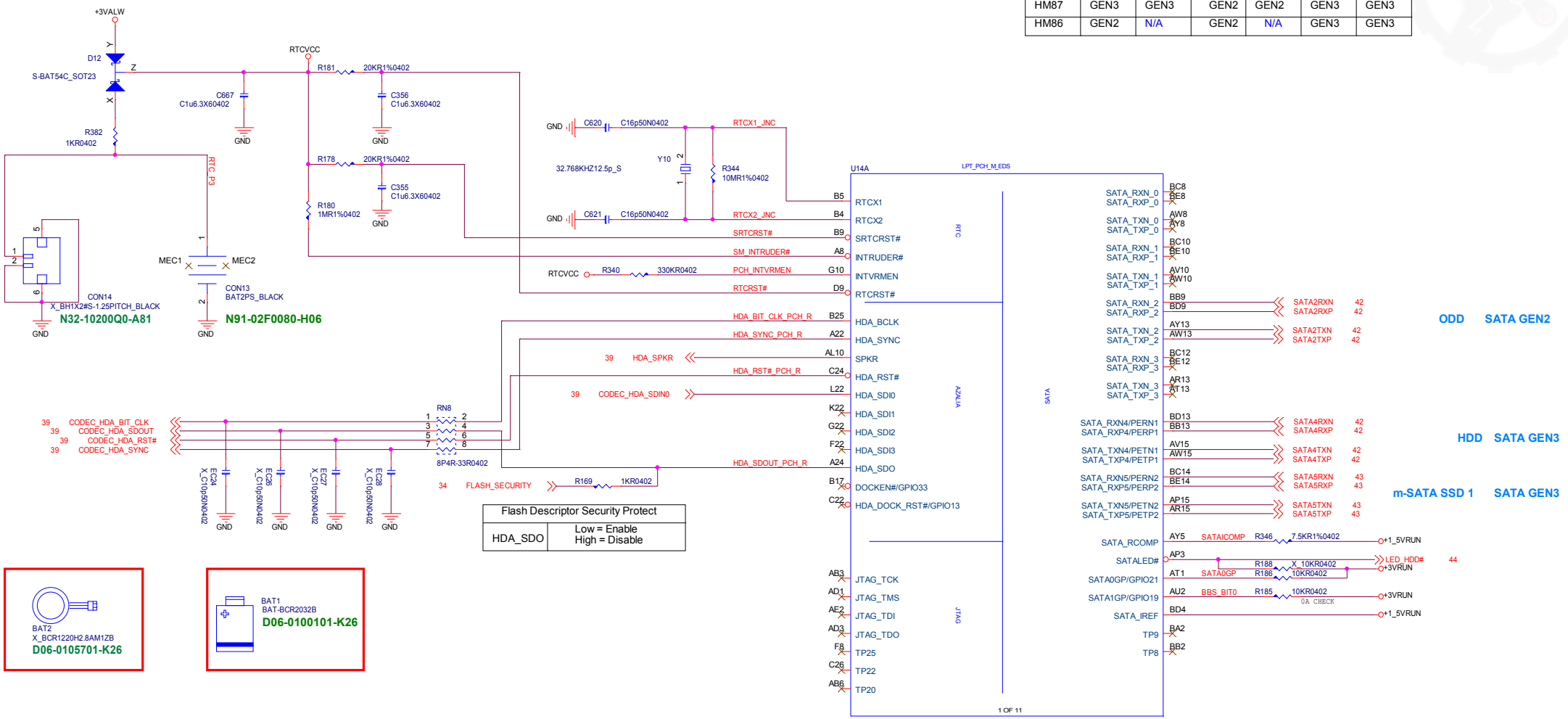
Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

BAT2
X_BCR1220H2.8AM1ZB
D06-0105701-K26

BAT1
BAT-BCR2032B
D06-0100101-K26

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.

Title: PCH-1 (HDA/JTAG/SATA)

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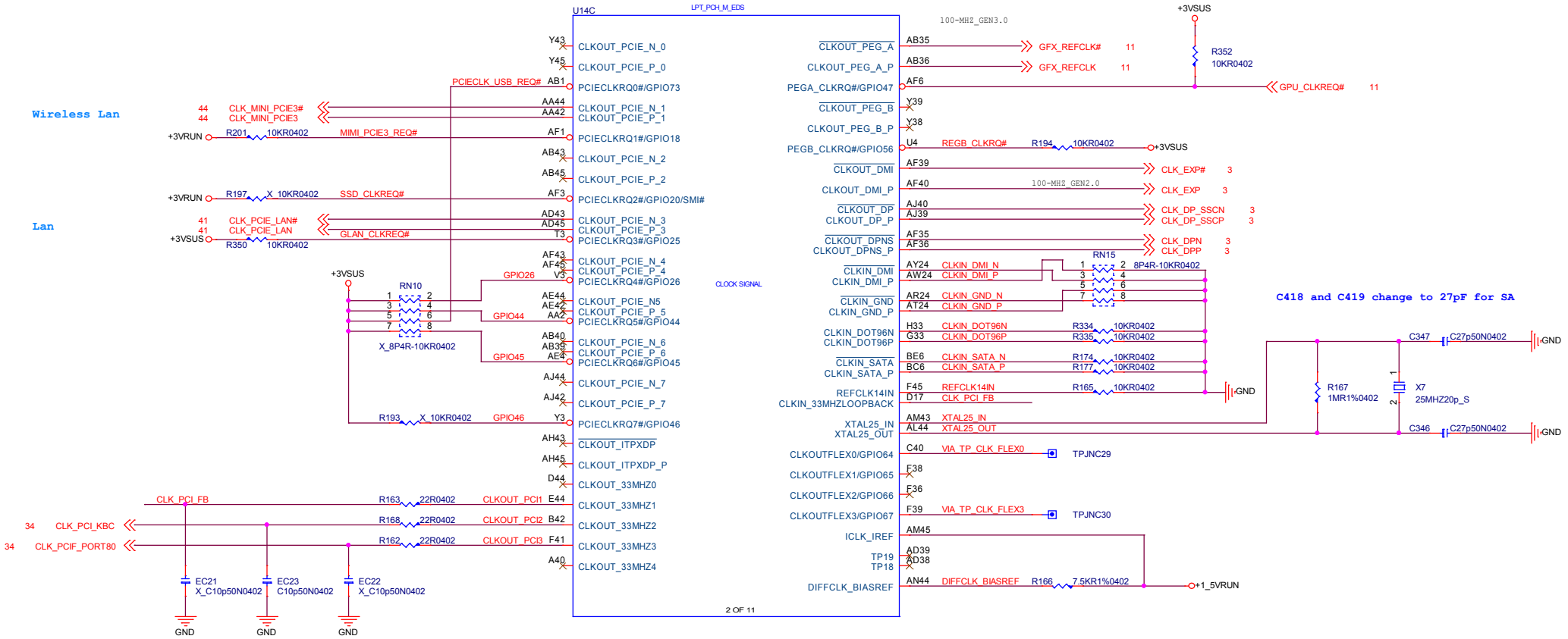
Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 k Ω ±10% external pull-up resistor instead of No Connect.

Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.

Title	PCH-2 (CLK)	
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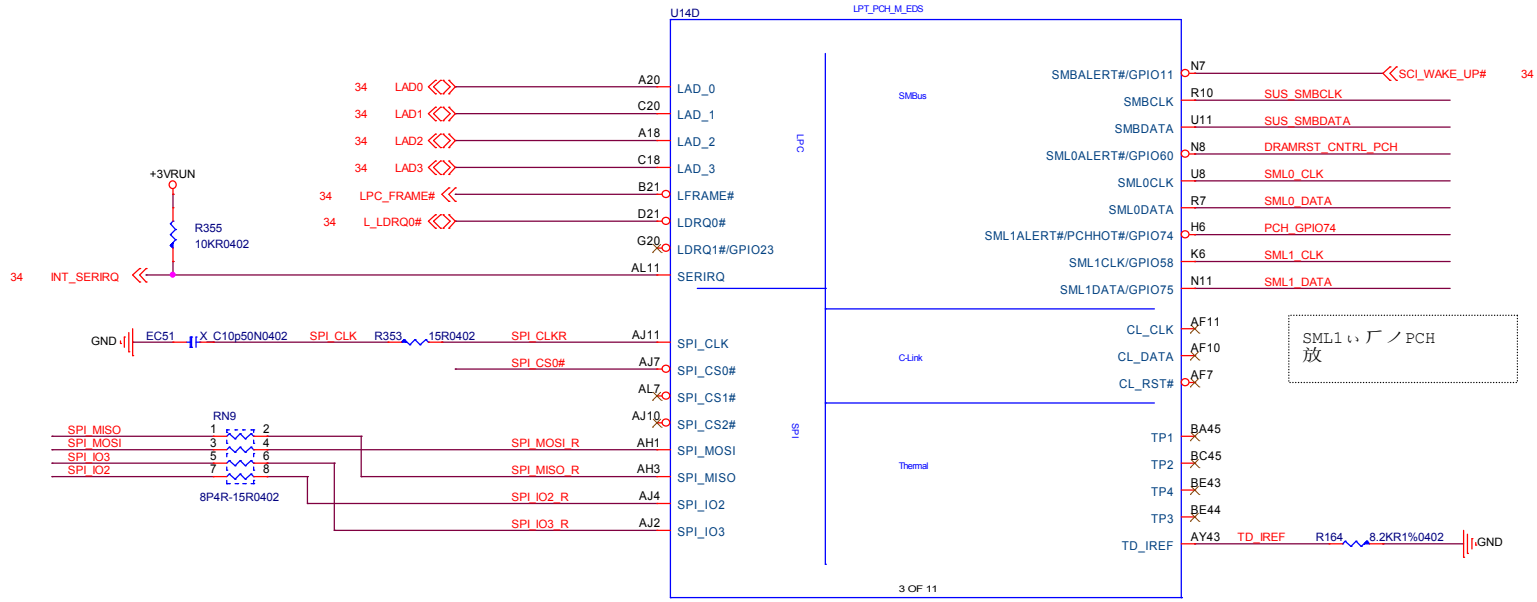
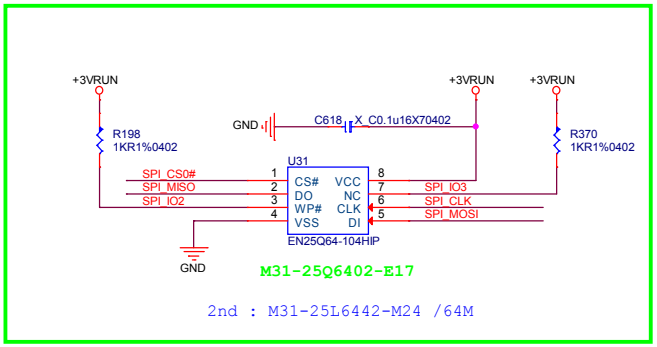
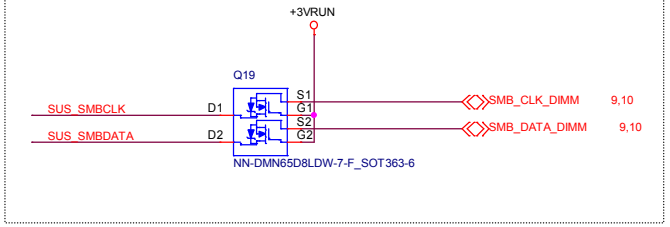
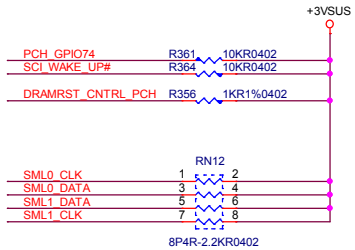
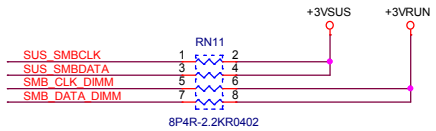
Lynx Point (LPC,SMBUS)











MICRO-STAR INT'L CO.,LTD.

Title: PCH-3 (LPC,SMBUS)

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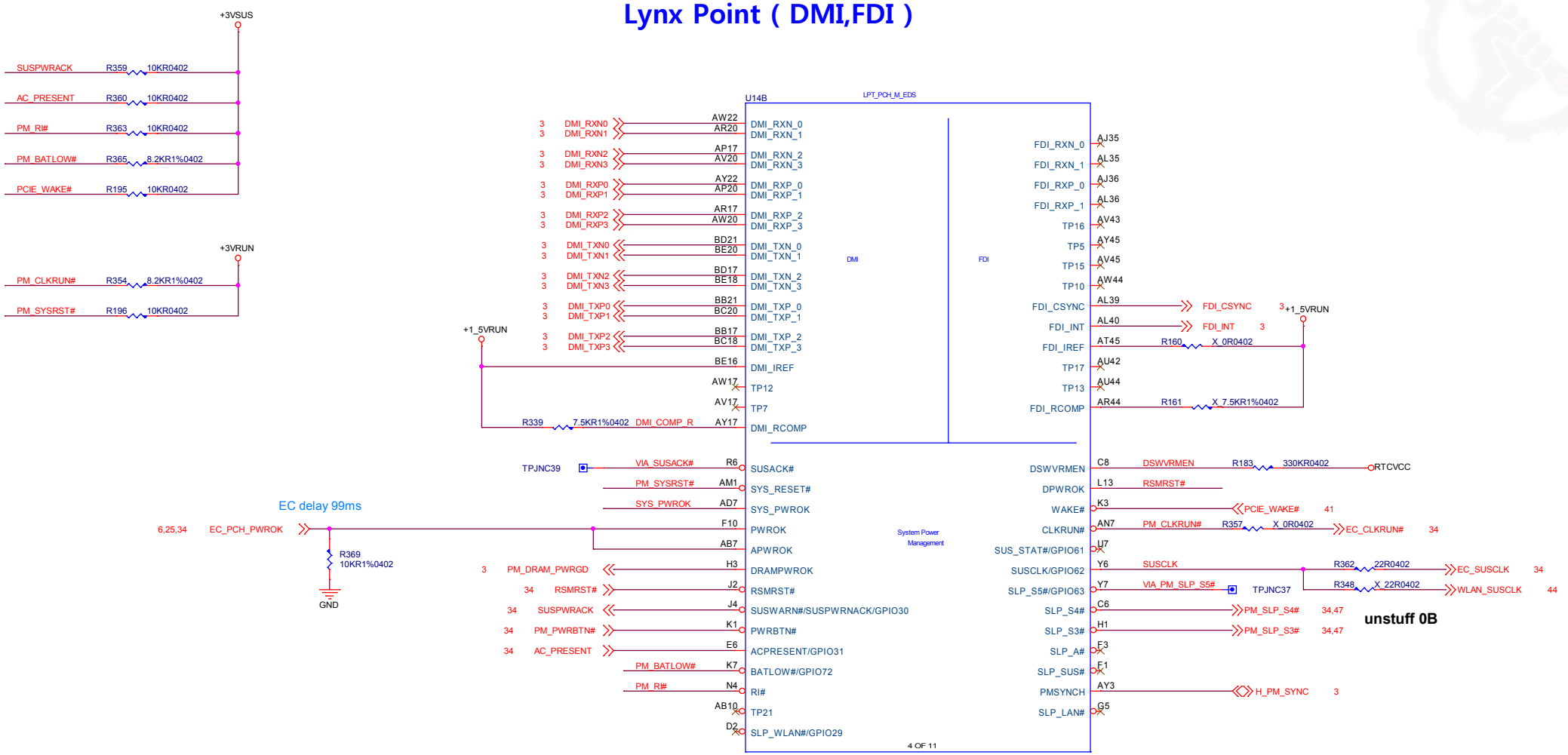
Lynx Point (DMI,FDI)



APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

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Title: PCH-4 (DMI,FDI)

Size: | Document Number: MS-16J3 | Rev: 1.0

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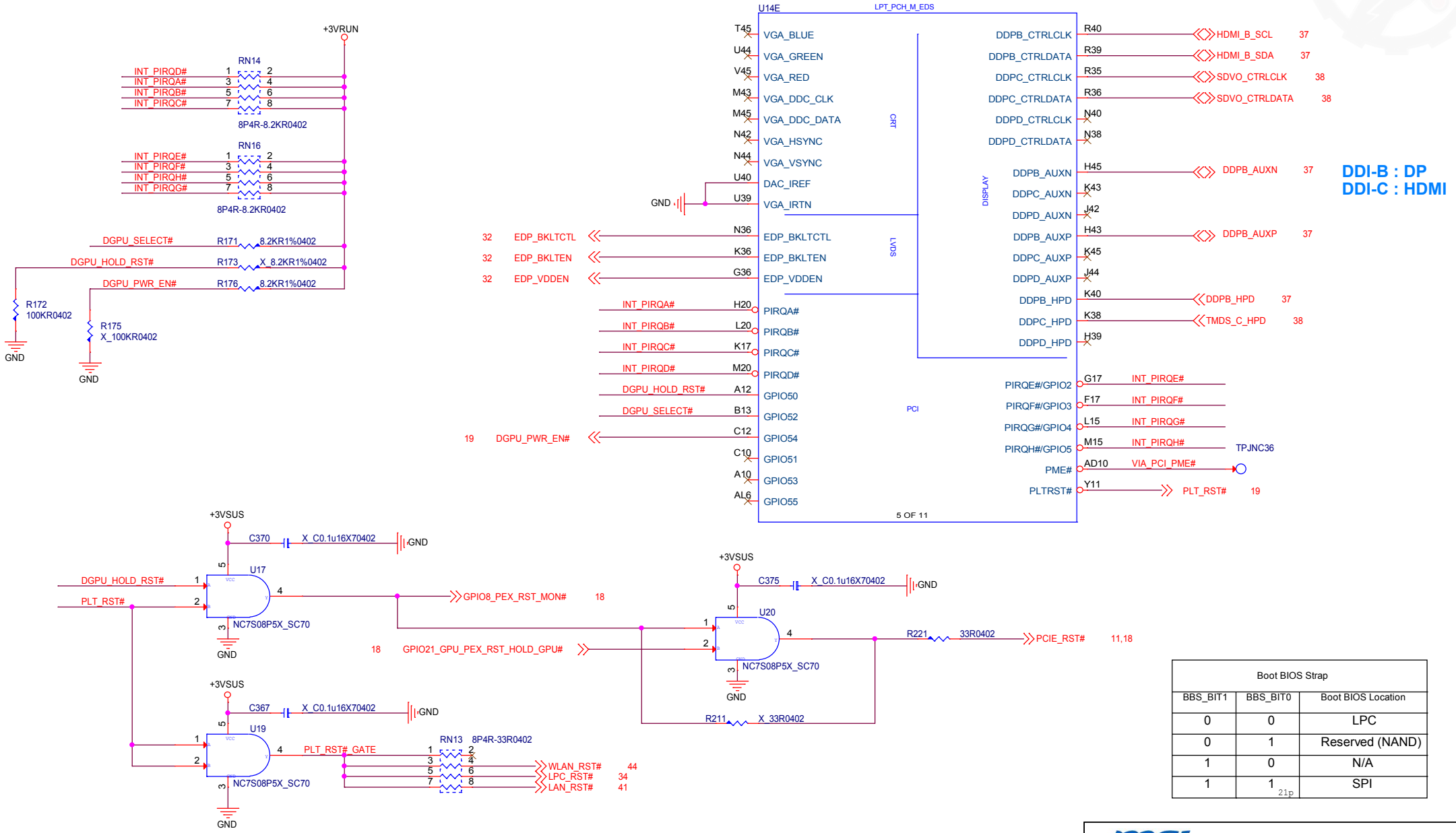
Lynx Point (PCI,DDI)



Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

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Title: PCH-5 (PCI,DDI)

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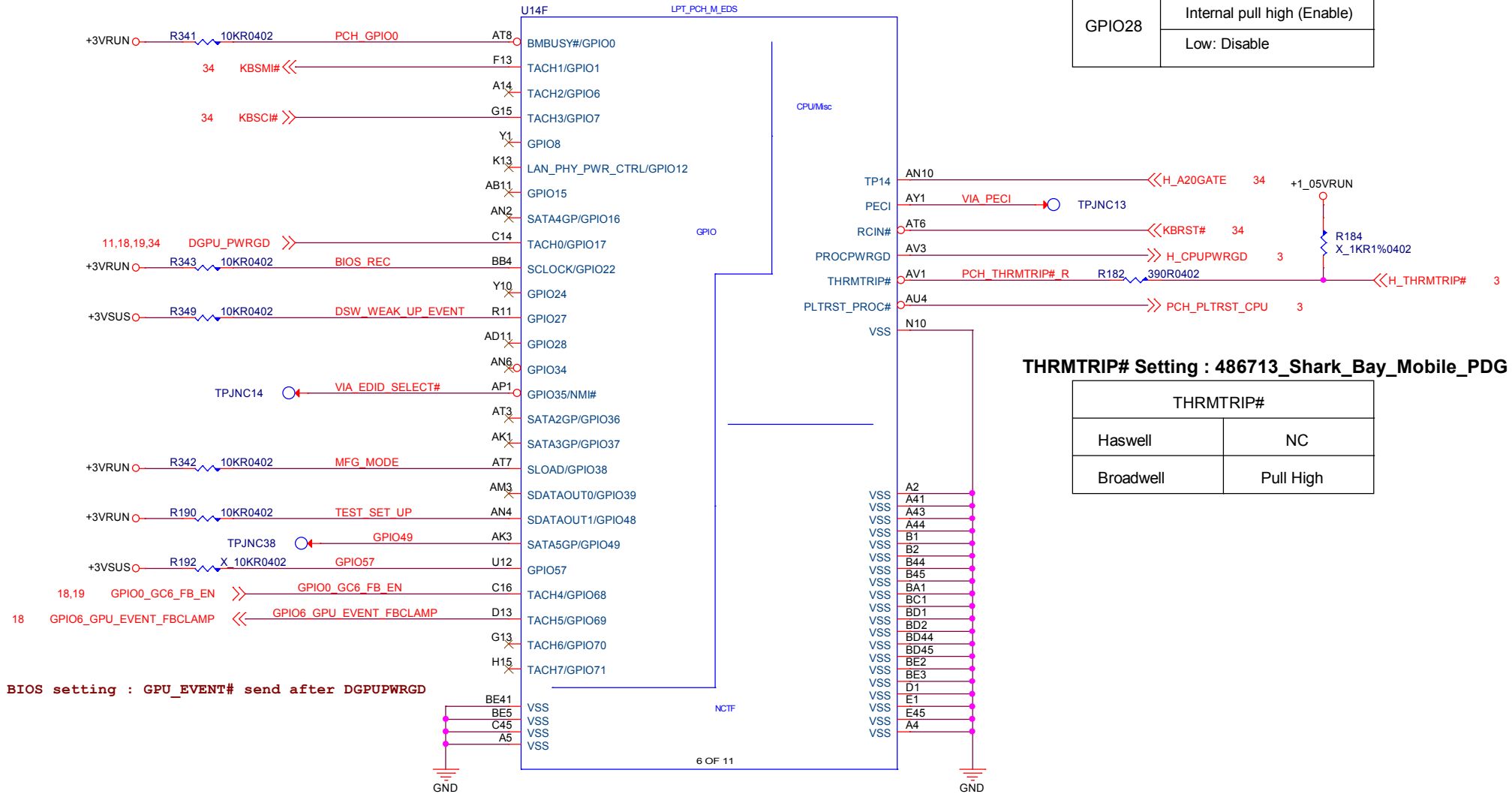
Lynx Point (GPIO,MISC)



BIOS setting : GPU_EVENT# send after DGPUPWRGD

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

THRMTRIP# Setting : 486713_Shark_Bay_Mobile_PDG

THRMTRIP#	
Haswell	NC
Broadwell	Pull High

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Title: PCH-6 (GPIO,MISC)

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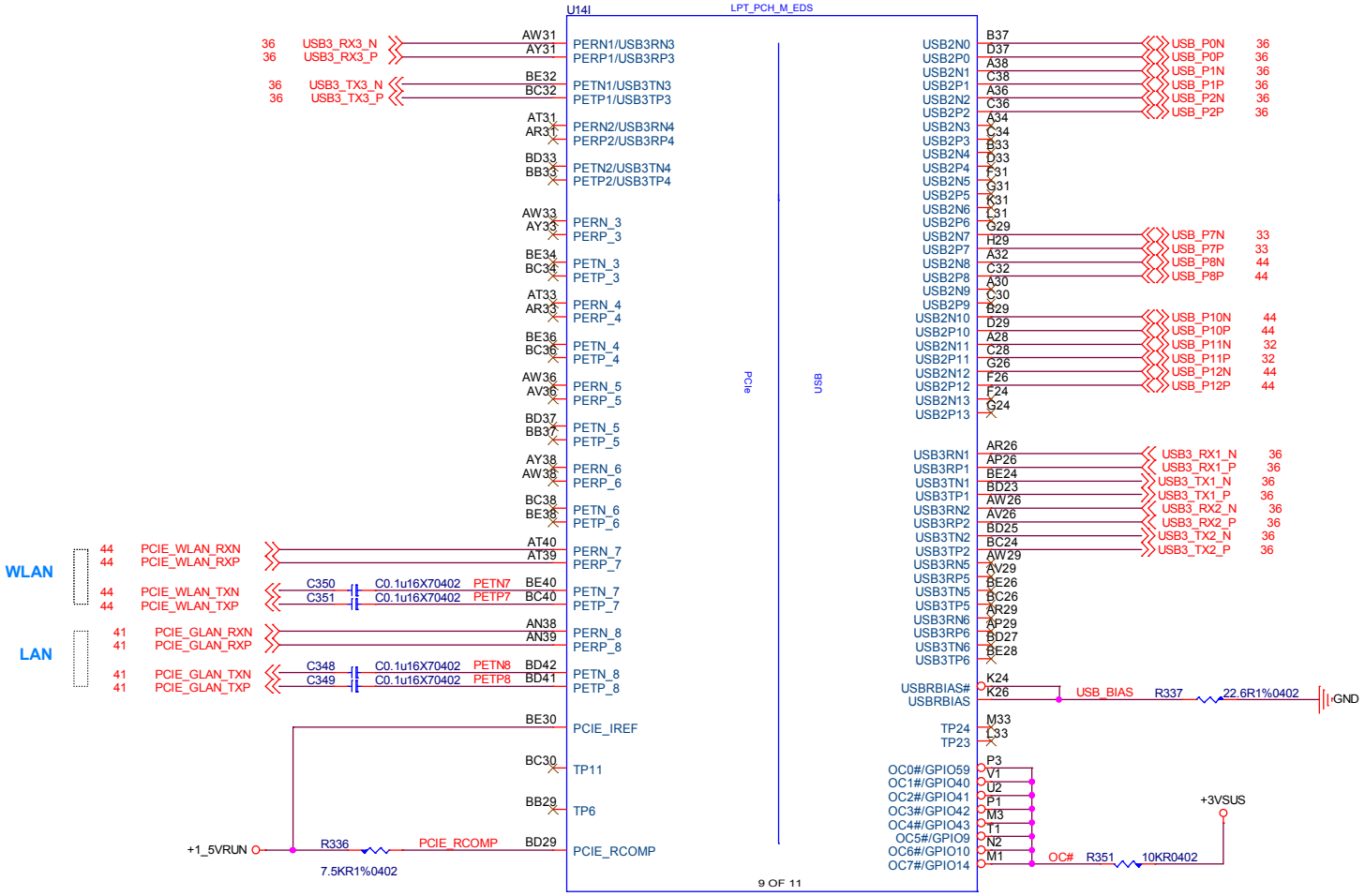
Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug transport 惠钡Port1 or Port9



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16J31
1	2	USB 3.0 Port 2	16J31
2	3	USB 3.0 Port 3	16J31
3			
4			
5			
6			
7		EPF021	
8		USB 2.0	16J12
9			
10		WLAN	
11		WebCam	
12		CARDREADER	16J12
13			

USB 2.0	USB 3.0
0	1
1	2
2	3
3	4
8	5
9	6

SKU	High Speed USB 3.0 I/O Ports					
	USB 3.0-1	USB 3.0-2	USB 3.0-3	USB 3.0-4	USB 3.0-5	USB 3.0-6
HM87	USB 3.0	USB 3.0	USB 3.0 / PCI-E	USB 3.0 / PCI-E	USB 3.0	USB 3.0
HM86	USB 3.0	USB 3.0	USB 3.0 / PCI-E	USB 3.0 / PCI-E	N/A	N/A

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Title: PCH-7 (PCIE,USB)

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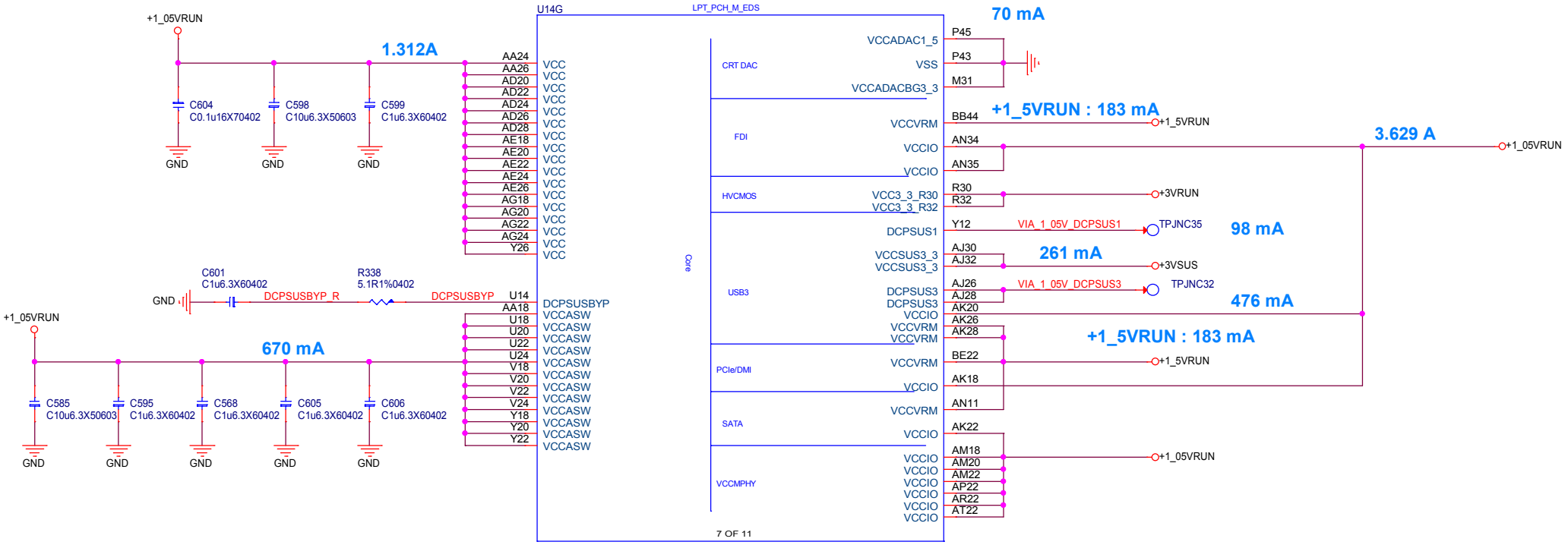
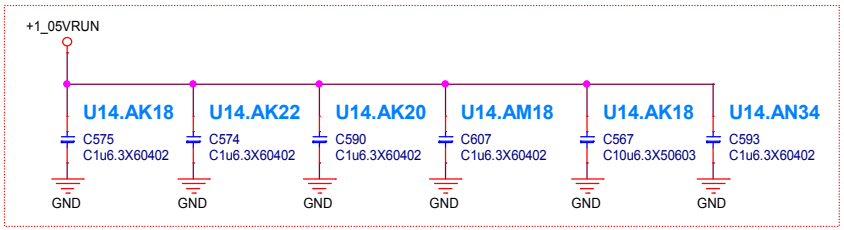
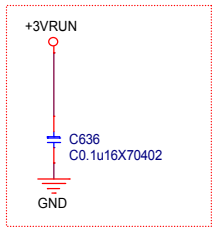
Lynx Point (Power)







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Title: PCH-8 (Power)

Size | Document Number: MS-16J3 | Rev: 1.0

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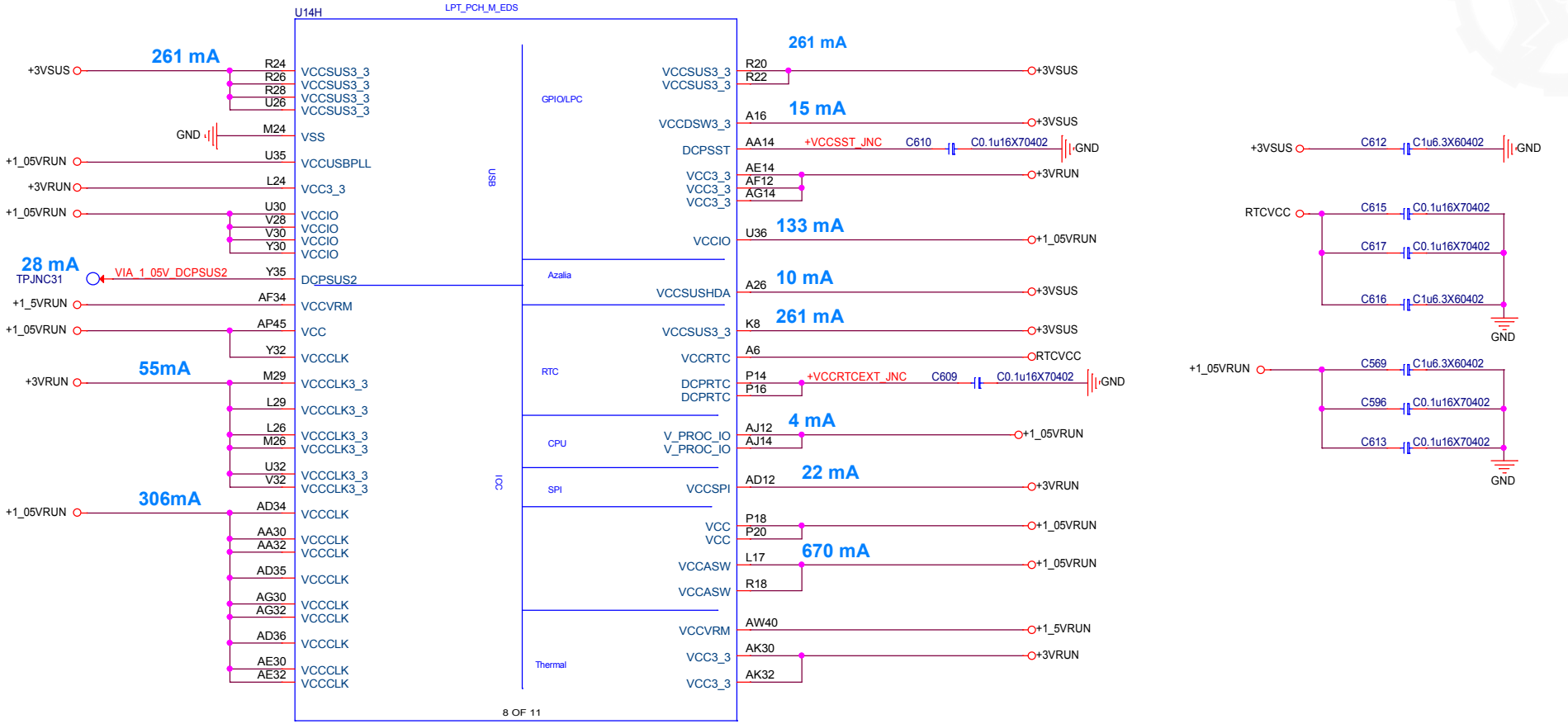
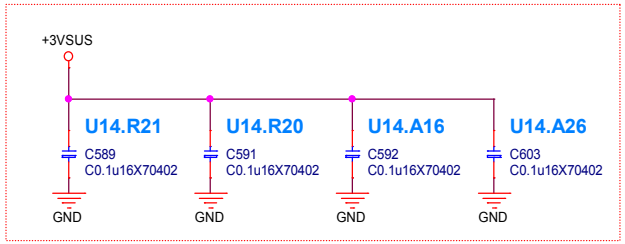
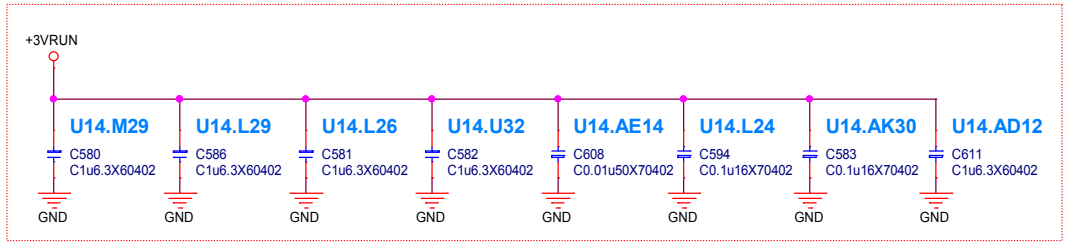
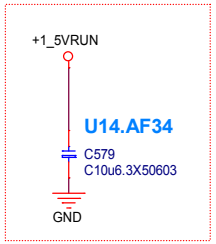
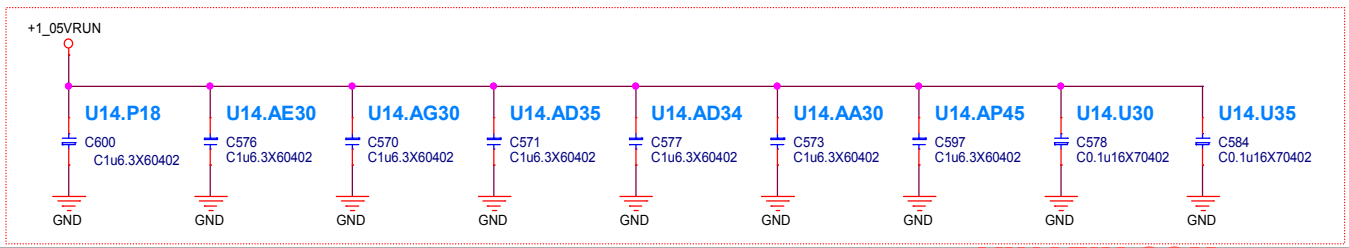
Lynx Point (Power)











MICRO-STAR INT'L CO.,LTD.

Title: PCH-9 (Power)

Size | Document Number: MS-16J3 | Rev: 1.0

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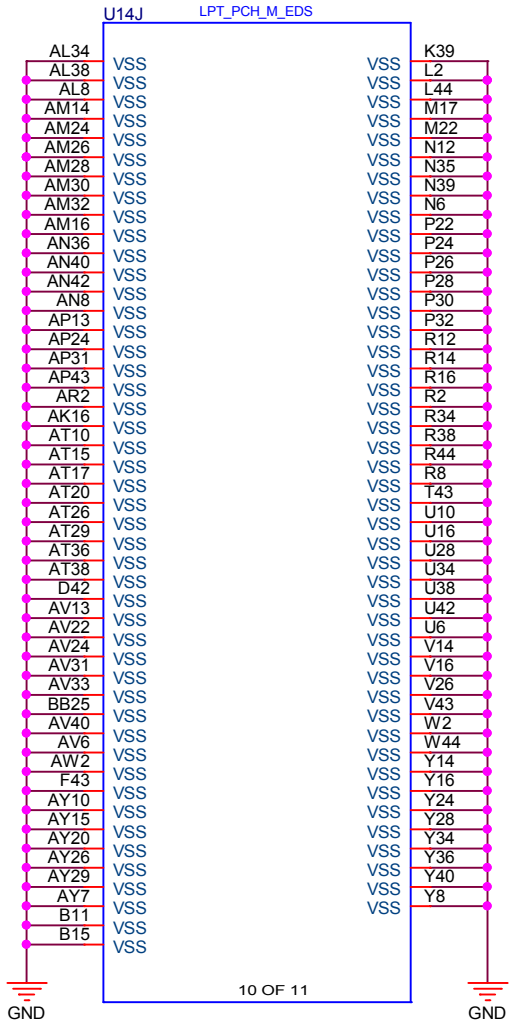
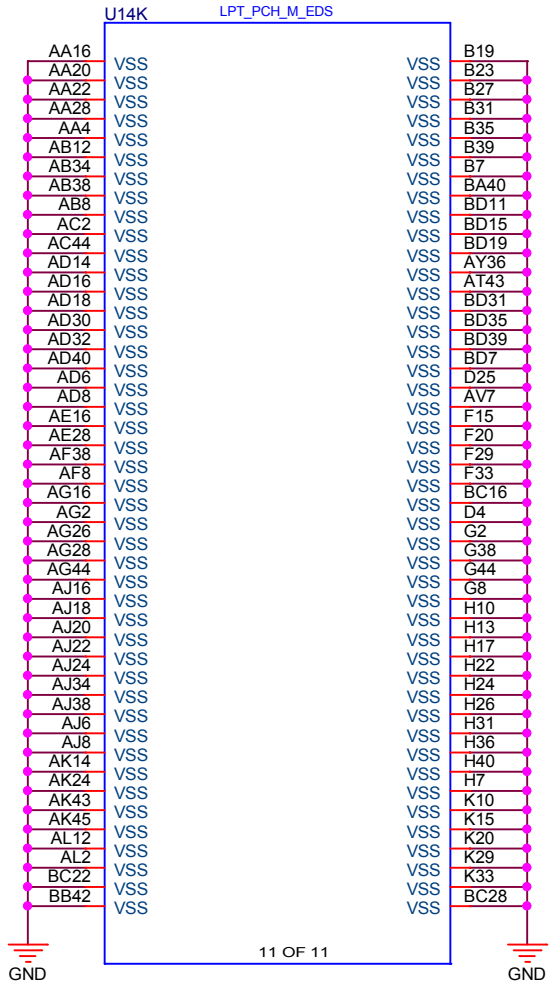
Lynx Point (GND)





MICRO-STAR INT'L CO.,LTD.

Title: PCH-10 (GND)

Size | Document Number: MS-16J3 | Rev: 1.0

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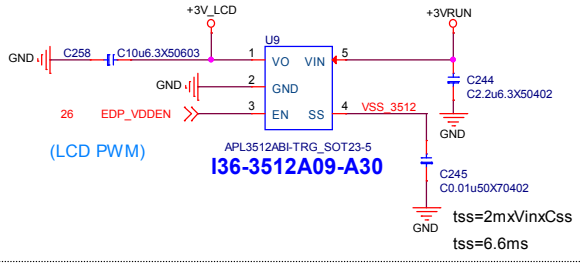
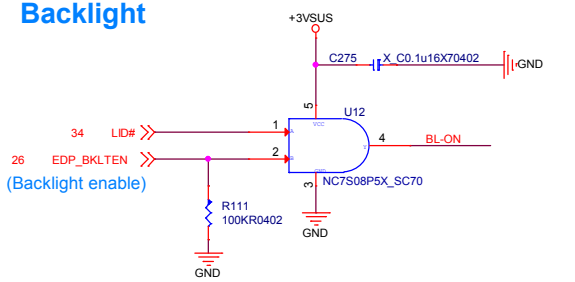
eDP

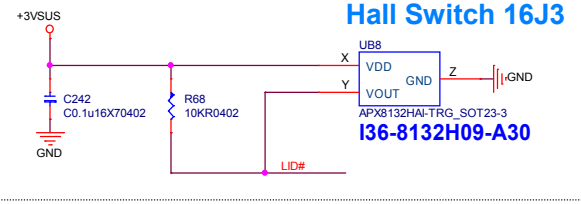
Pannel Device Logic Power



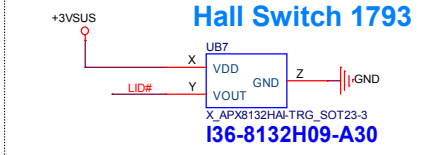
Backlight



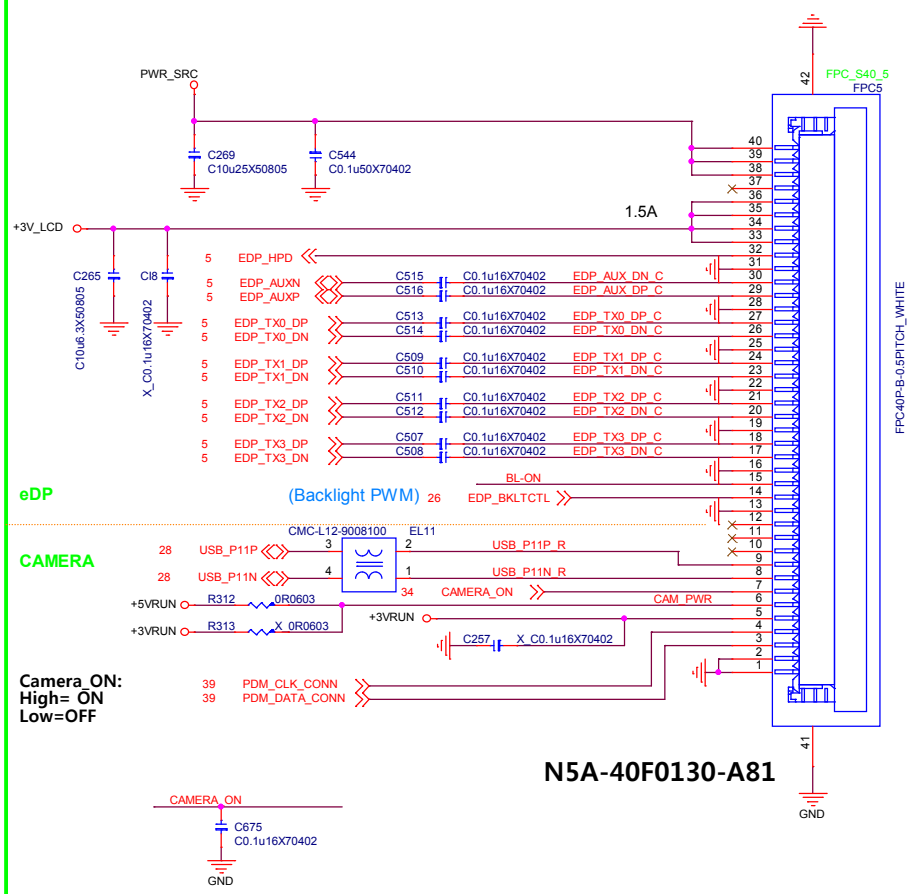
Hall Switch 16J3

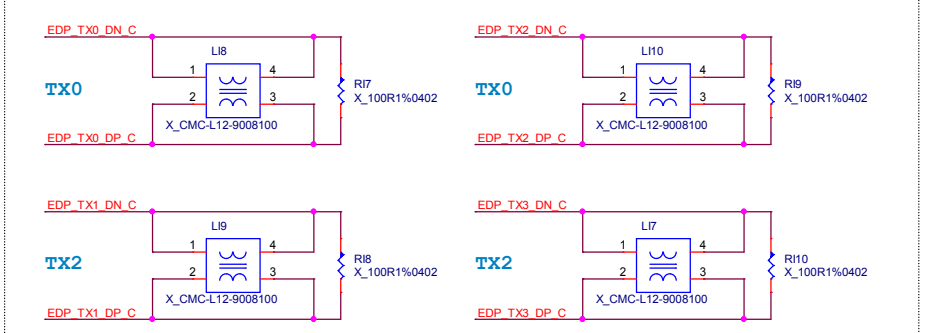


Hall Switch 1793



eDP CONN CAMERA





LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

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Title: eDP /Camera

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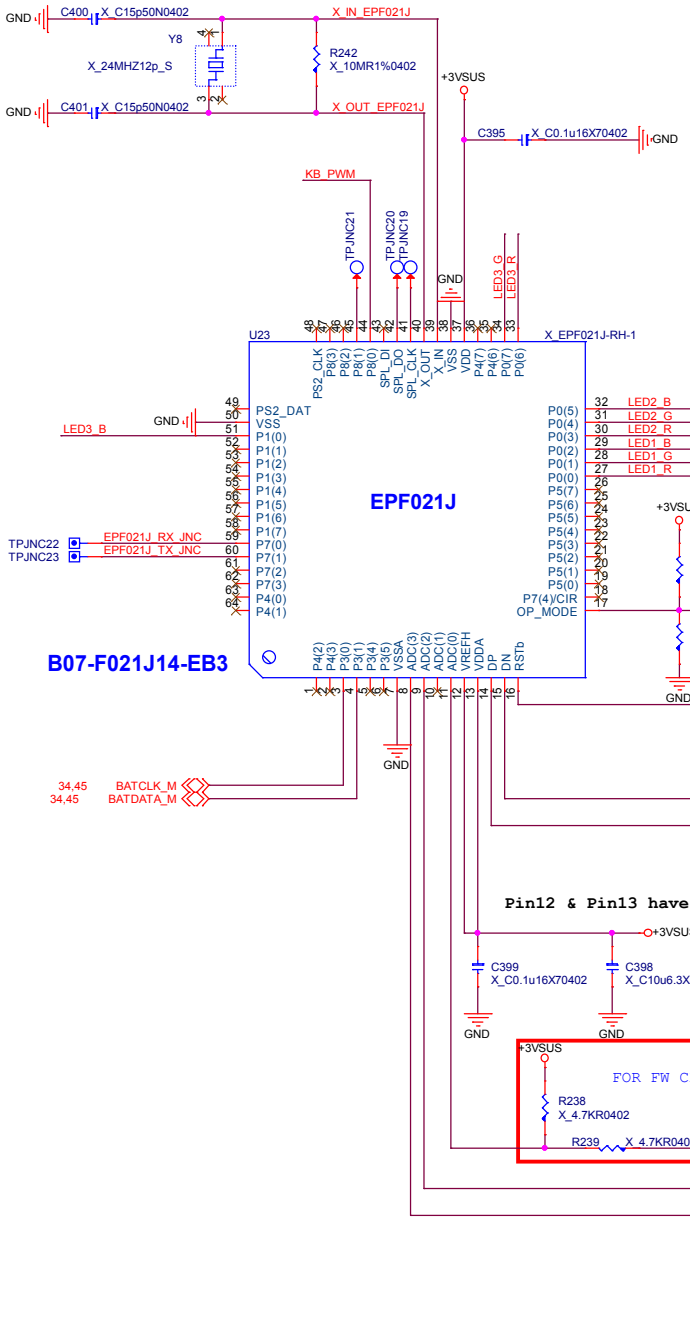
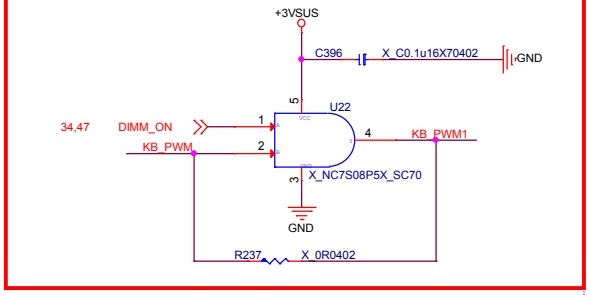
LED 8051 Controller

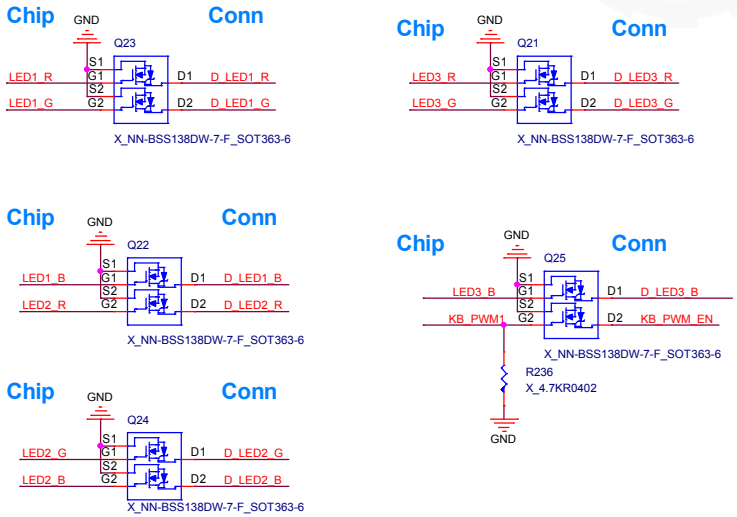
C749 and C750 change to 15pF for SA



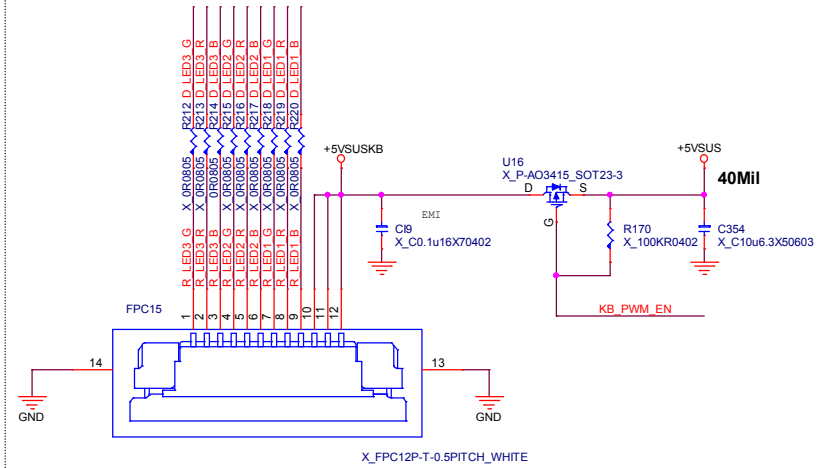
LED KB FLASH ERROR



EPF021J Sink current not enough, only using BSS138 (0.22A)



LED Keyboard CONN



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

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Title: LED_8051

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KBC(KB3930QFB1)

Hardware Reset

ED before RC

RC and R Close SW

SW9, SW-TACTB1-4PS, RST_SW#, R222 47KR1%0402, ED19 ESD-SFI0402-050E101NP, C377 C0.1u16X70402, R223 33R0402, EC_RST#

SW Debug (LPC)

CON12, BH1X14HS-1.25PITCH_WHITE

N32-1140060-H06

HW Debug

SW10, PWR_SW#, C671 X_C0.1u16X70402, X_SW-TACTB1S

R45 10KR0402, C145 C0.1u16X70402

ROM

AVL : M31-2551232-GA0

U34, MX25L512EMI-10G

M31-2551222-M24

ALLSYSPG

JNC20, JNC18, JNC19, X_0402

EC_ALLSYSPG 37,51

U1 — KB3930QFB1-B1

LPC I/F: SERIRQ, LFRAME#, PCICLK, CLKRUN#/GPIO1D, LAD0, LAD1, LAD2, LAD3

ECRST#, KBRST#, SCI#/GPIO0E, GA20, PCIRST#

FAN&PWM: PWM0/GPIO0F, PWM1/GPIO10, GPIO11/PWM2, GPIO19/PWM3, FANPWM0/GPIO12, FANPWM1/GPIO13, FANFB0/GPIO14, FANFB1/GPIO15

IKB: KSO0/GPIO20/TP_TEST, KSO1/GPIO21/ITP_PLL, KSO2/GPIO22/TP_ANA_TEST, KSO3/GPIO23/TP_ISP, KSO4/GPIO24, KSO5/GPIO25, KSO6/GPIO26, KSO7/GPIO27, KSO8/GPIO28, KSO9/GPIO29, KSO10/GPIO2A, KSO11/GPIO2B, KSO12/GPIO2C, KSO13/GPIO2D, KSO14/GPIO2E, KSO15/GPIO2F/E51_RXD(ISP), KSO16/GPIO48, KSO17/GPIO49, KSI0/GPIO30/E51TXD(ISP), KSI1/GPIO31, KSI2/GPIO32, KSI3/GPIO33, KSI4/GPIO34/EDI_CS, KSI5/GPIO35/EDI_CLK, KSI6/GPIO3/EDI_DIN, KSI7/GPIO37/EDI_DO

ESB: GPIO0B/ESB_CLK, GPIO0C/ESB_DAT_O/ESB_DAT_I

CIR: GPIO40/CIR_RX/AD6, GPIO41/CIR_RLC_TX/AD7, GPIO0A/RLC_RX2, GPIO0D/RLC_TX2

SPI FLASH: MISO, MOSI, SPICLK/GPIO58, SPICS#

PS2 I/F: PSCLK2/GPIO4E, PSDAT2/GPIO4F, PSCLK1/GPIO4C, PSDAT1/GPIO4D, PSCLK0/GPIO4A/P80CLK, PSDAT0/GPIO4B/P80DAT

UART: E51TXD/GPIO16, E51RXD/GPIO17

XCLKI, XCLKO, V18R

POWER/GROUND: VCC, AVCC, AGND, GND

SMBUS: SDA0/GPIO45, SCL0/GPIO44, SDA1/GPIO47, SCL1/GPIO46

AD/DA: DA0/GPO3C, DA1/GPO3D, DA2/GPO3E, DA3/GPO3F, AD0/GPI38, AD1/GPI39, AD2/GPI3A, AD3/GPI3B, AD4/GPI42, AD5/GPI43

SDI: GPXIOA00/SDICS#, GPXIOA01/SDICLK, GPXIOA02/SDIMOSI

GPXIOA03, GPXIOA04, GPXIOA05, GPXIOA06, GPXIOA07, GPXIOA08, GPXIOA09, GPXIOA10, GPXIOA11, GPXIOD0, GPXIOD1, GPXIOD2, GPXIOD3, GPXIOD4, GPXIOD5, GPXIOD6, GPXIOD7/PECI

GPIO04, GPIO07/I_clk_8051, GPIO08/I_clk_peri, GPIO18, GPIO50, E51CS#/GPIO52, E51TMR0/GPIO54/WDT_LED#, E51INT1/GPIO56, GPIO57/XCLK32K, GPIO59/TEST_CLKSPICLKI

LED: GPIO1A/NUMLED#, E51TMR1/GPIO53/CAPSLED#, E51INT0/GPIO55/SCROLED#

B02-0393024-E18

EC_PROTECT_PWR=>OD pin

Pin 105-108 8mA-16mA Sink

Pin 92 16mA-20mA Sink

Pin 39,91 16mA-20mA Sink

Keyboard conn

CON5, FPC26P-T-1PITCH_WHITE

N5A-26F0270-A81

CNI8, CNI7, CNI10, CNI9 — 8p4C-100p50N0402

PU/PD

BATCLK_M R248 2.2KR1%0402

BATDATA_M R246 2.2KR1%0402

SMB_CLK_EC R234 2.2KR1%0402

SMB_DATA_EC R233 2.2KR1%0402

KBRST#, H_A20GATE

KBRST# R250 X_100KR0402

RSMRST# R187 10KR0402

MB_ID

PR121 100KR0402

MB_ID

R229 X_10KR1%0402

Title	KBC(KB3930QFB1)
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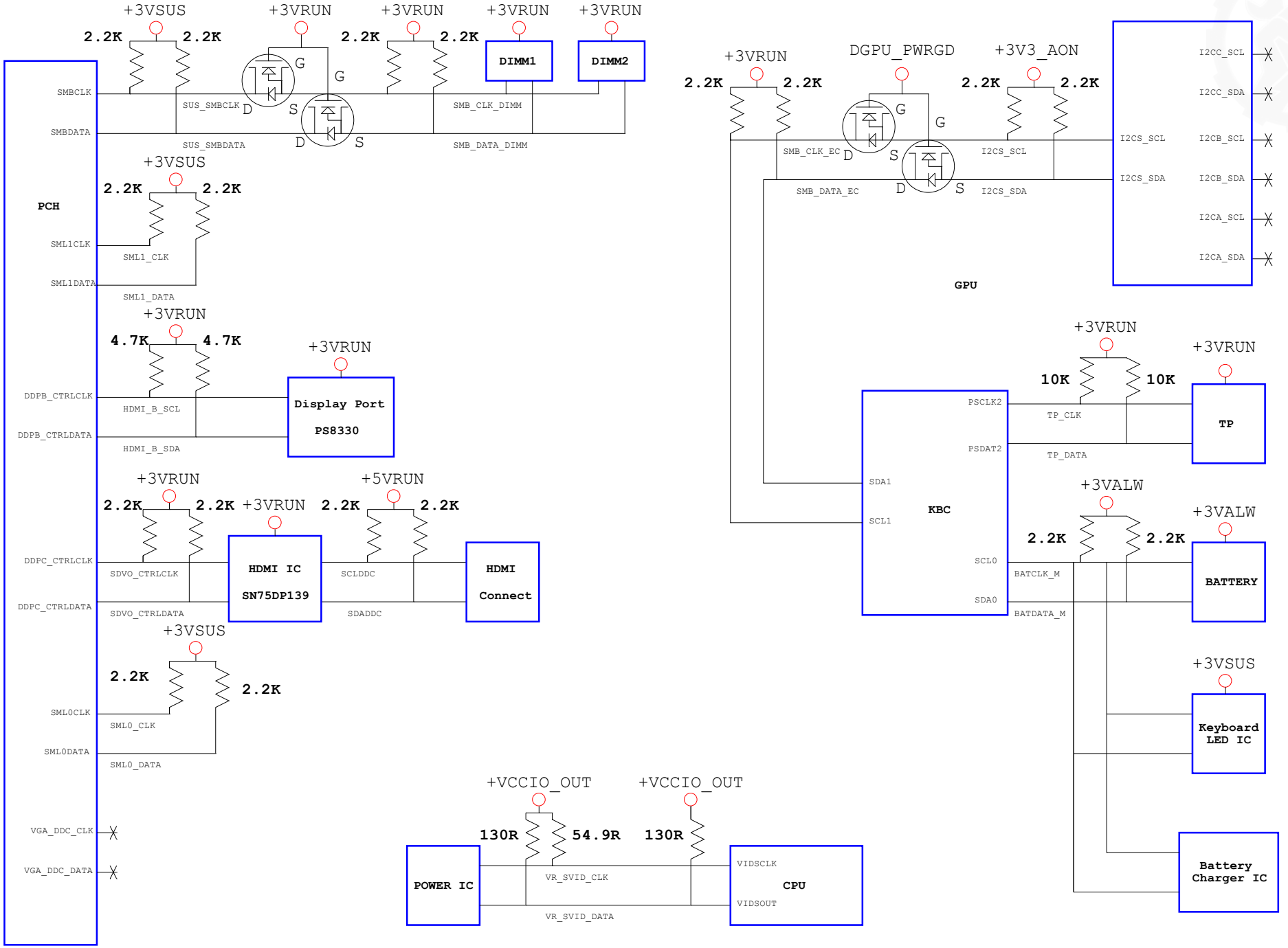

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Title: SMB Topology

Size: | Document Number: MS-16J3 | Rev: 1.0

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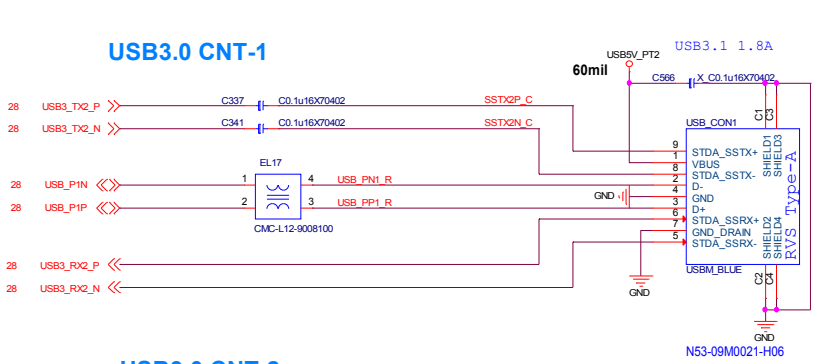
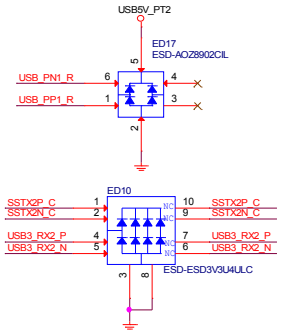
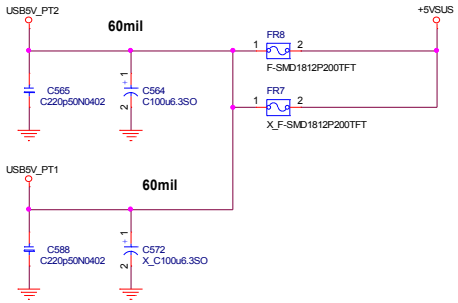
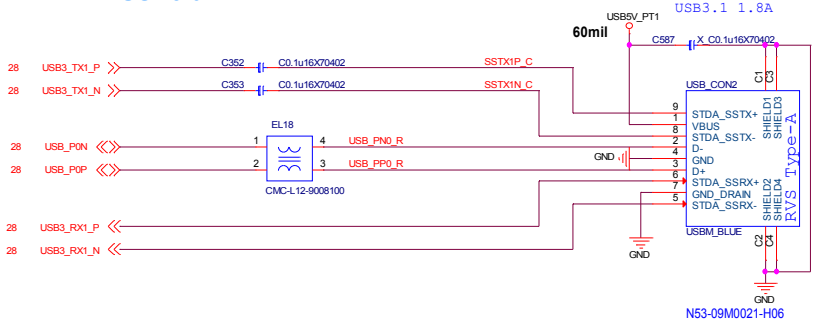
USB3.0 CNT-1

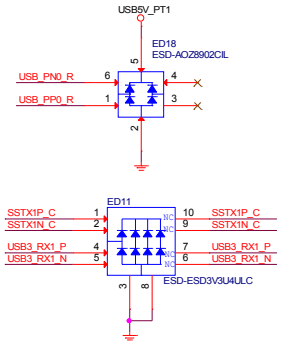




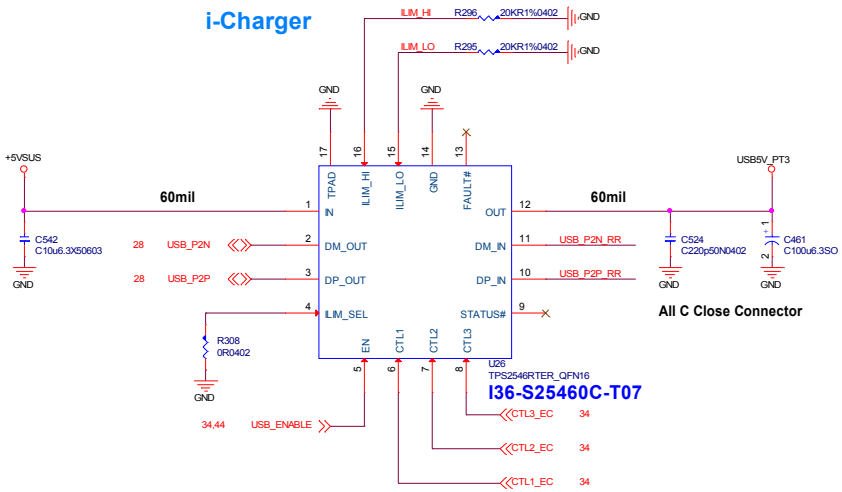


USB3.0 CNT-2

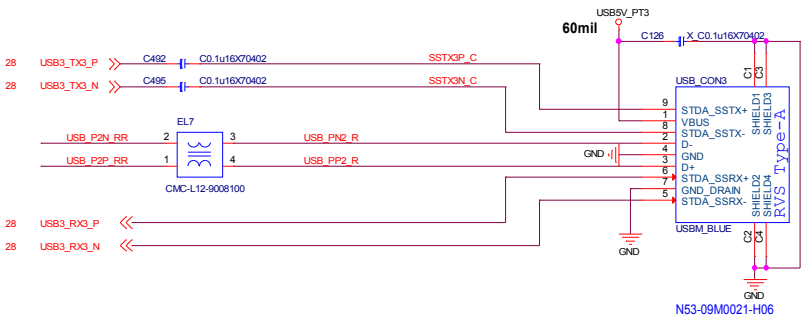


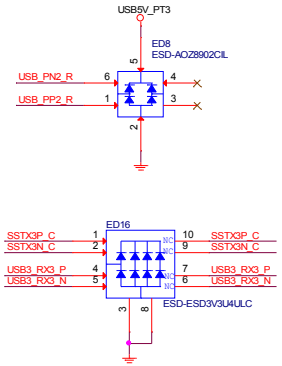


i-Charger



USB3.0 CNT-3





MSI	MICRO-STAR INT'L CO.,LTD.	
Title	USB 3.0 /iCharger	
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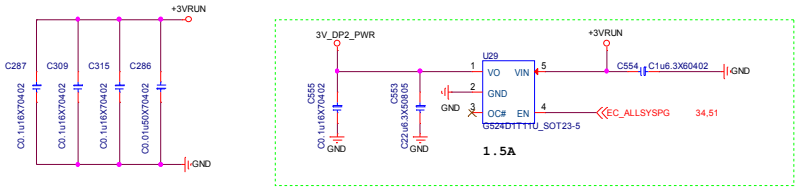
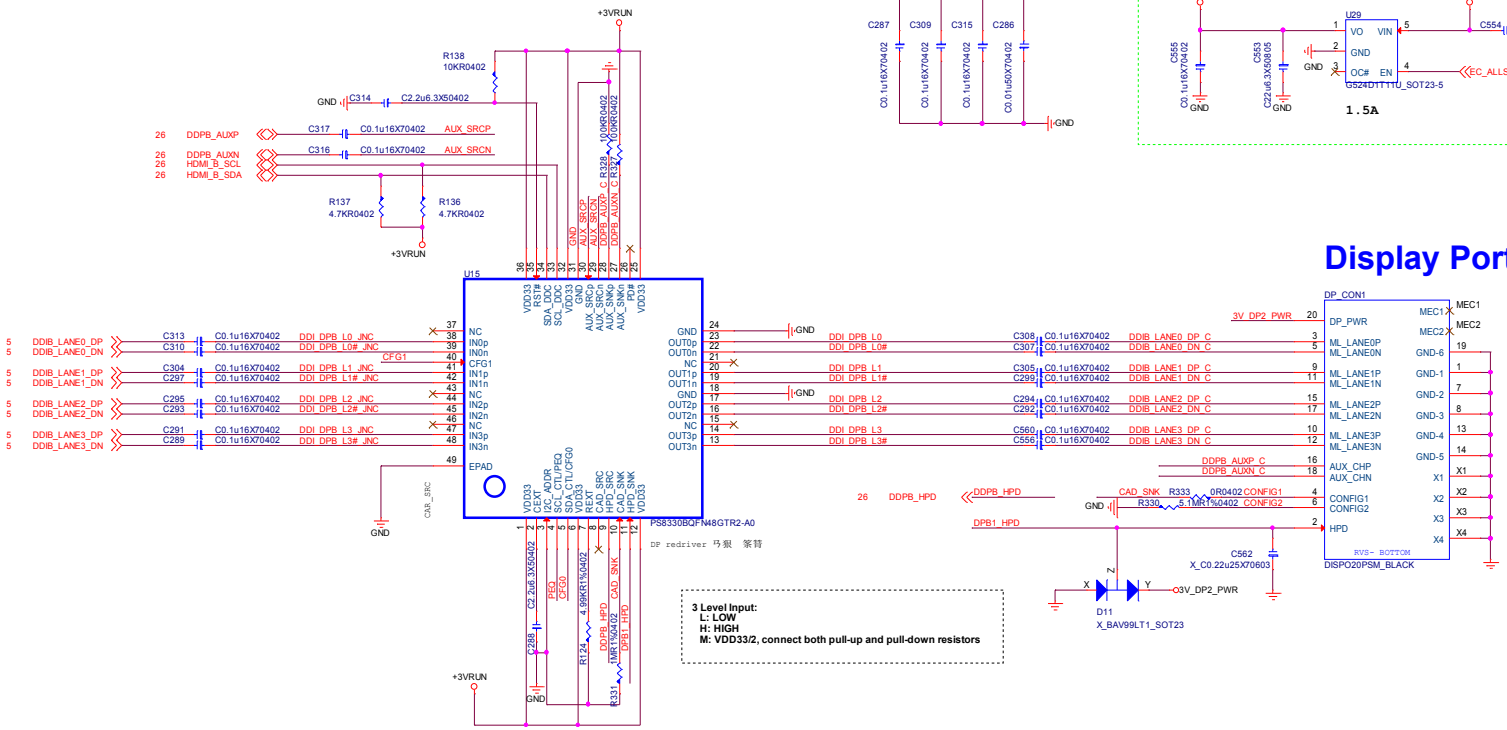
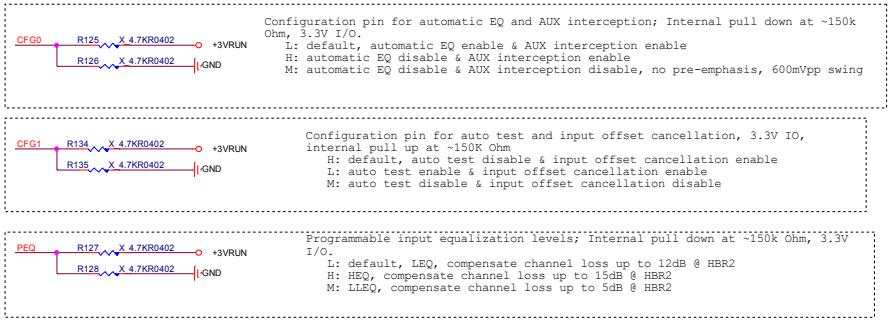
Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.

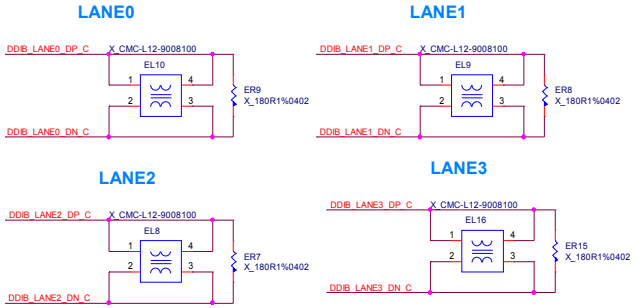




Display Port



EMI Close Connector



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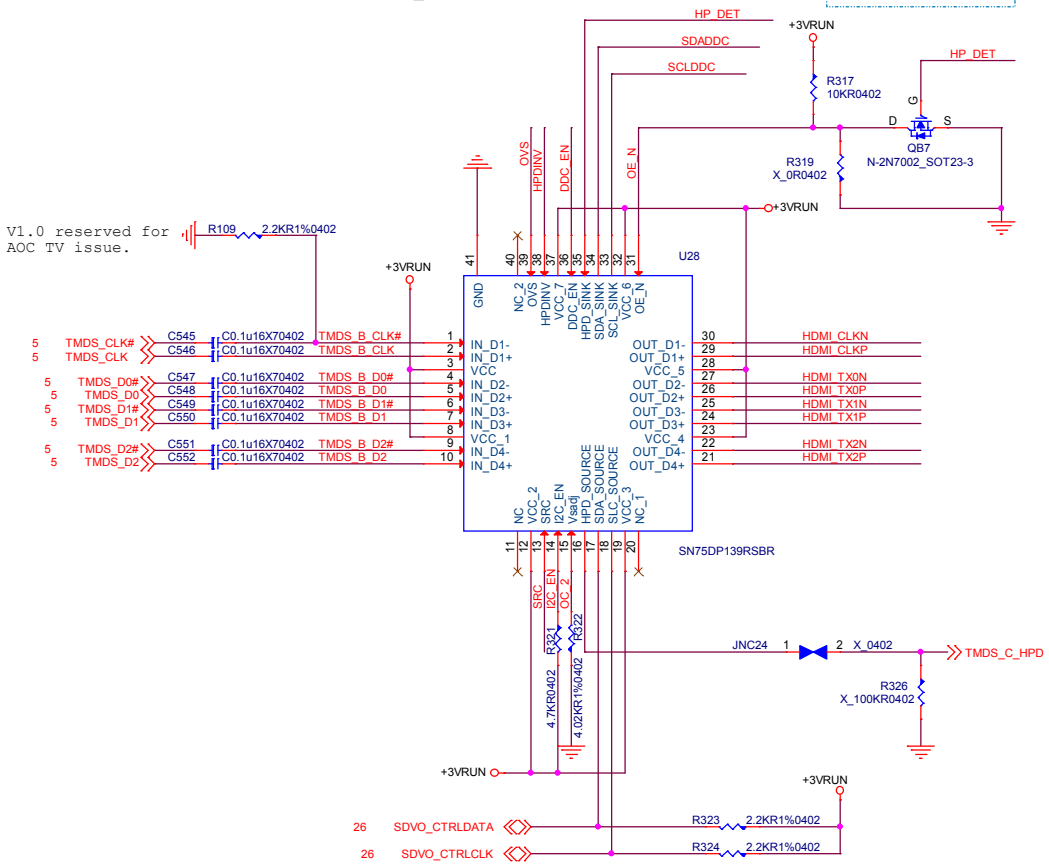
HDMI Level Shifter

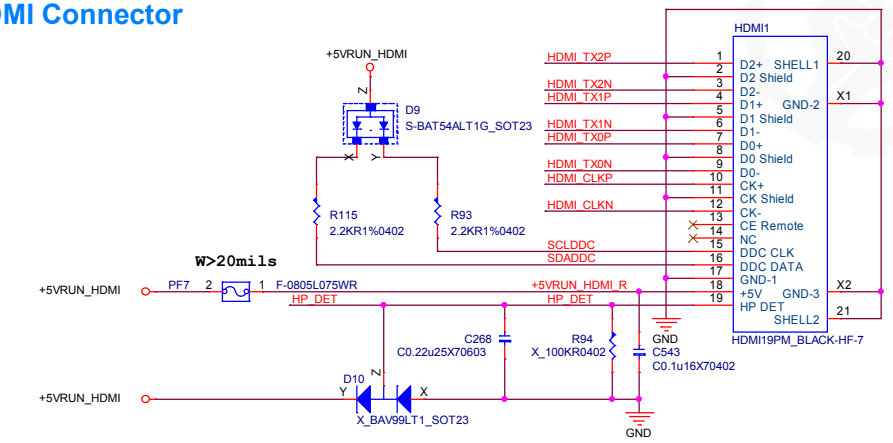
HP_DET
PLUGGED 5V
UNPLUGGED 0V

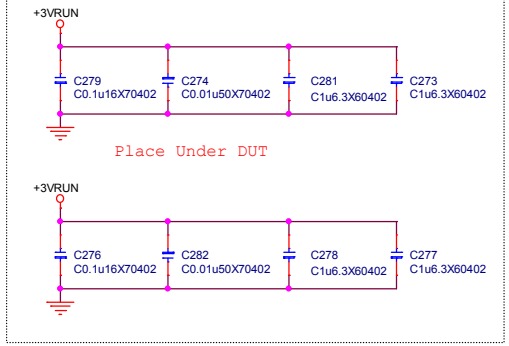
HPD_SNK Internal PD 130kohm ESD 10KV

V1.0 reserved for AOC TV issue.



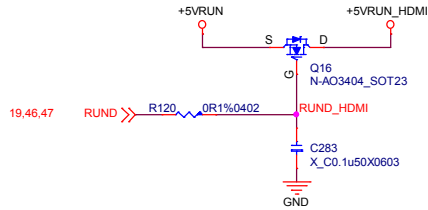
HDMI Connector

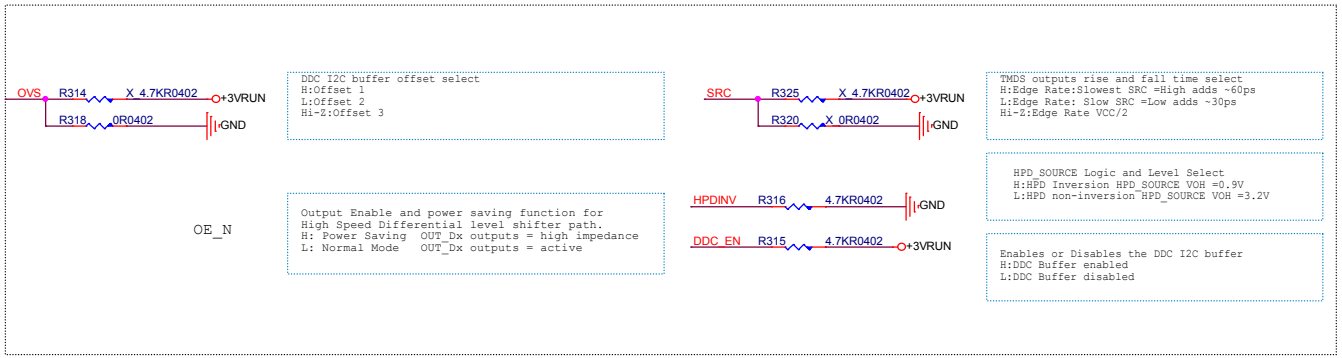




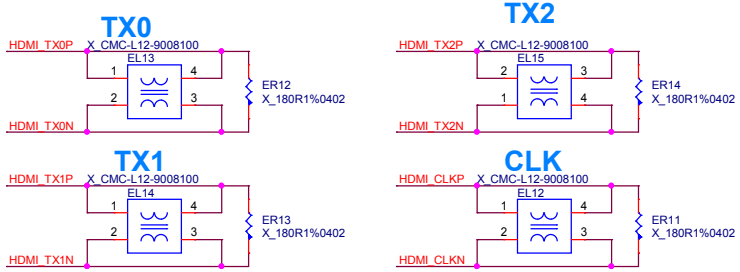
Avoid HDMI Leakage

W>20mils





EMI Close Connector



MICRO-STAR INT'L CO.,LTD.

Title: HDMI DP139

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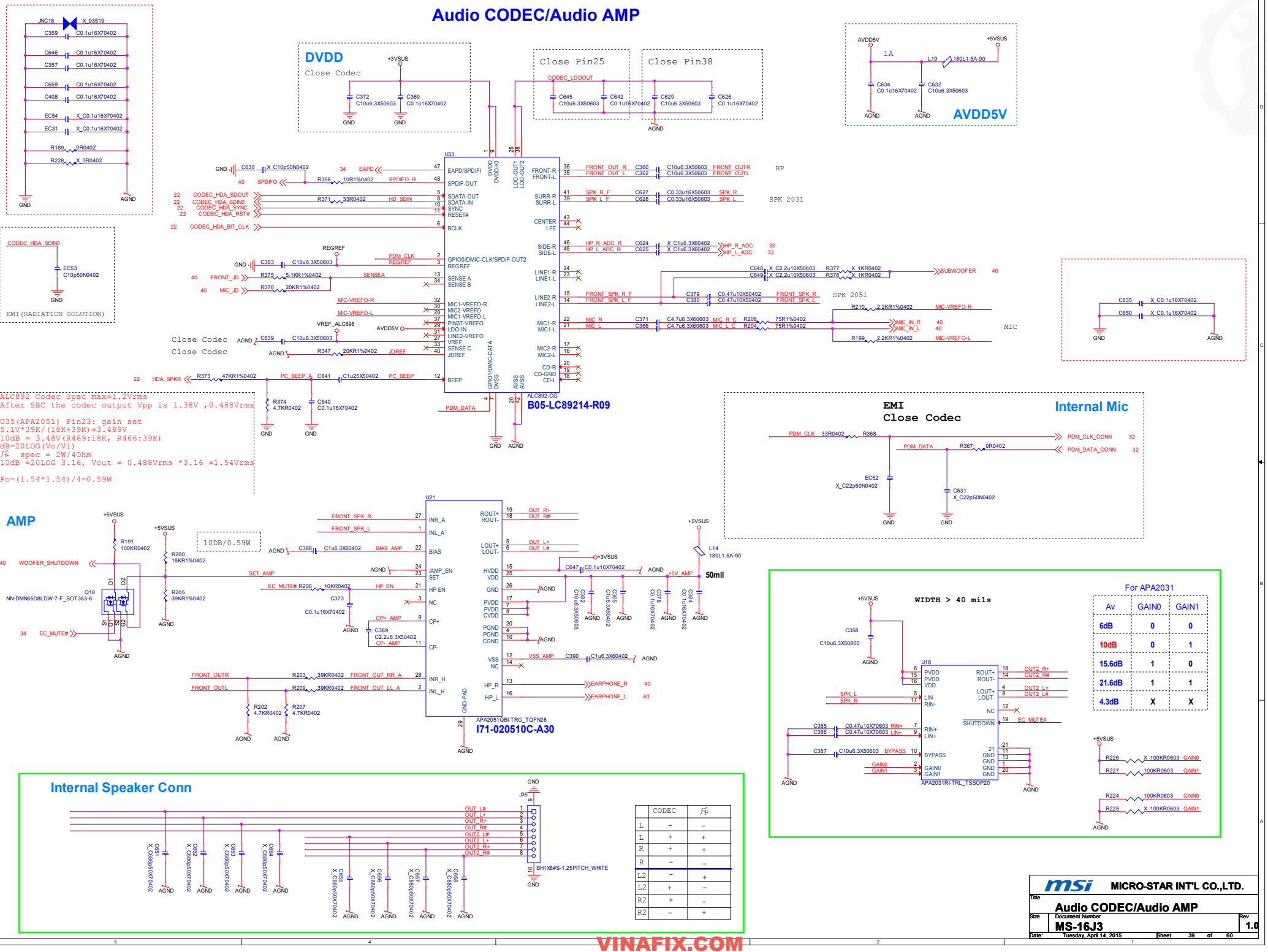
Audio CODEC/Audio AMP



Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

	CODEC	
L	-	-
L	+	+
R	+	+
R	-	-
L2	-	+
L2	+	-
R2	+	-
R2	-	+

MICRO-STAR INT'L CO.,LTD.

Title: Audio CODEC/Audio AMP

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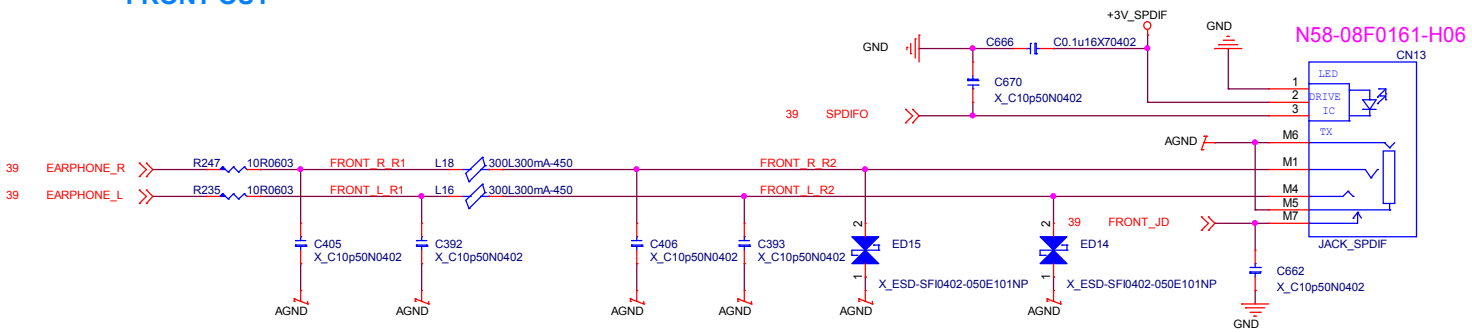
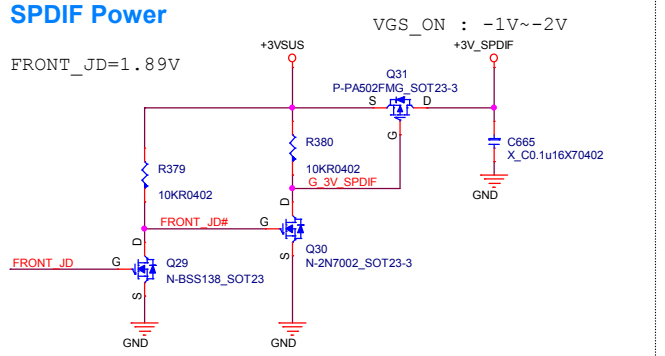
Audio CONN / Woffer

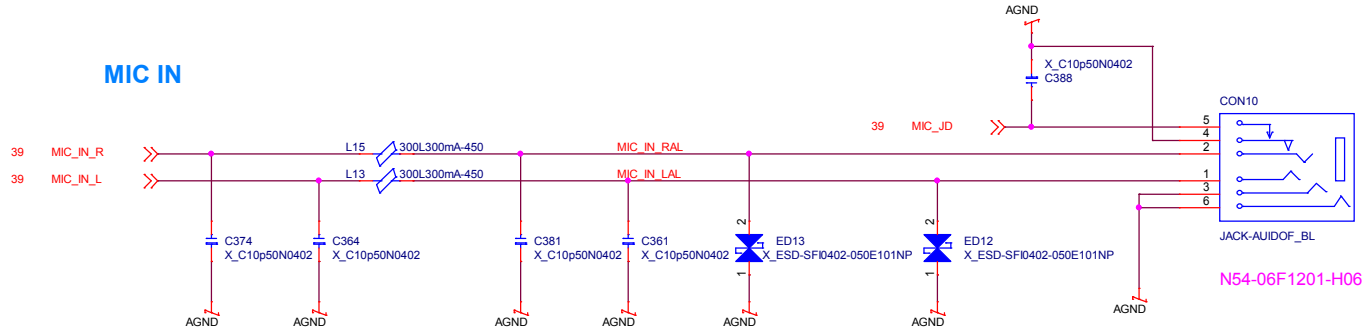
FRONT OUT

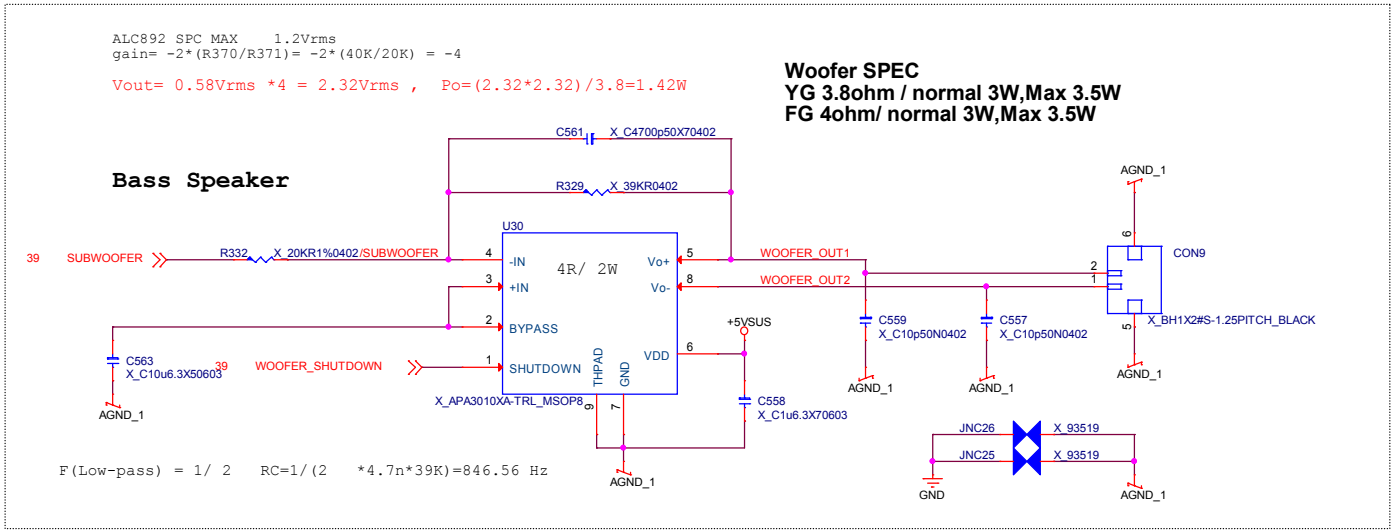


SPDIF Power



MIC IN





MICRO-STAR INT'L CO.,LTD.		
Title: Audio / Woffer		
Size	Document Number: MS-16J3	Rev: 1.0
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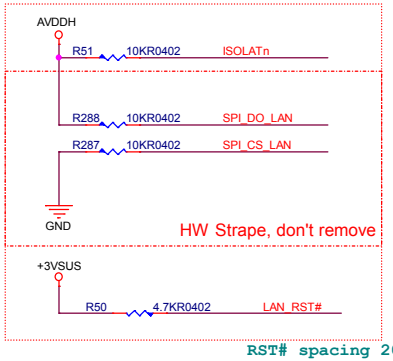
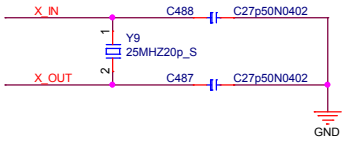
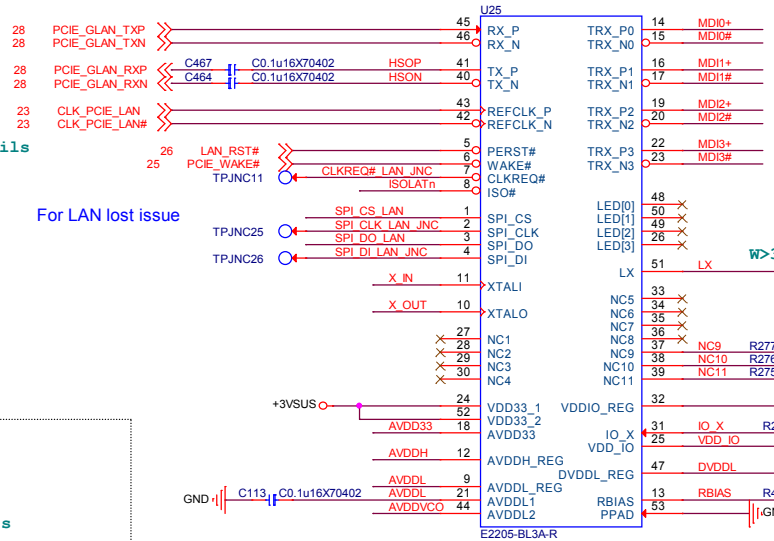
GIGA LAN(BigFoot BFN2205B)

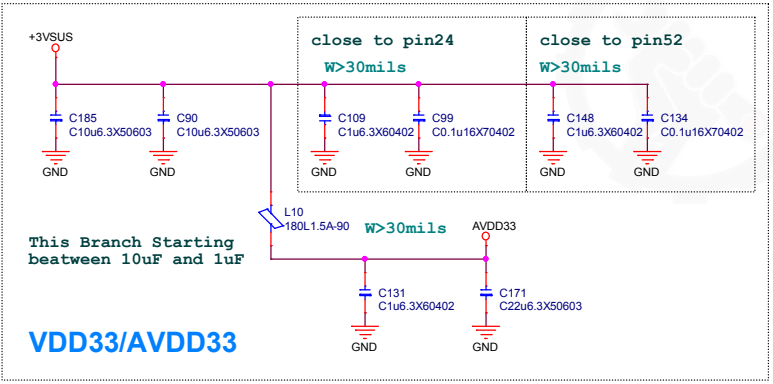




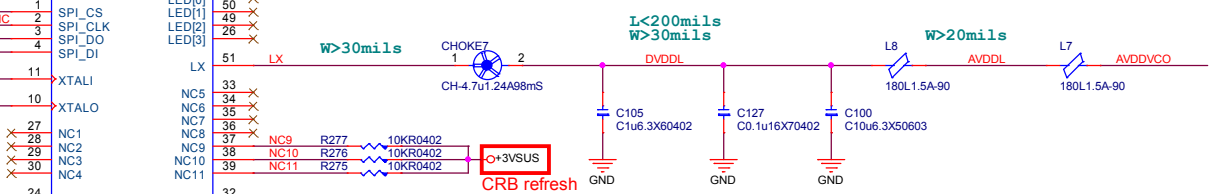
For LAN lost issue



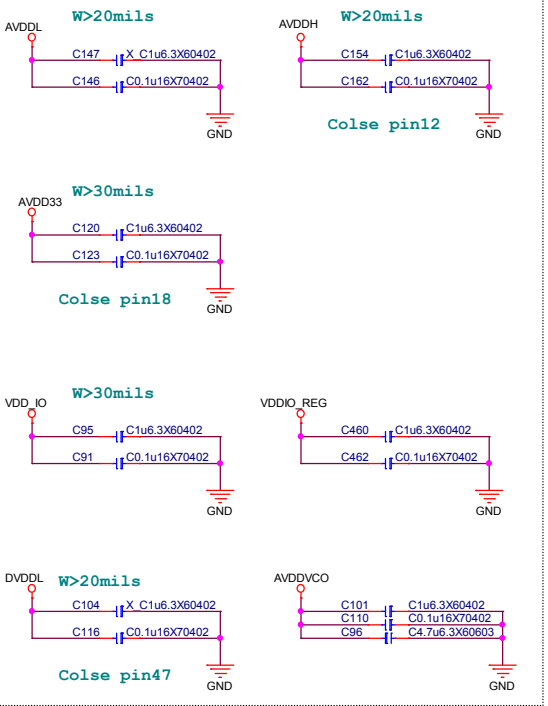
B06-E22050C-Q24

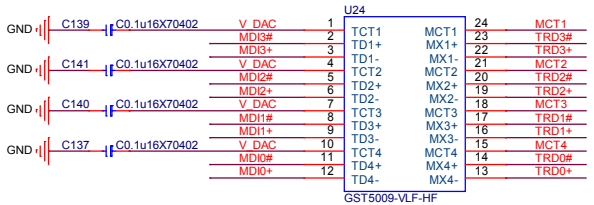


VDD33/AVDD33



Power CAP





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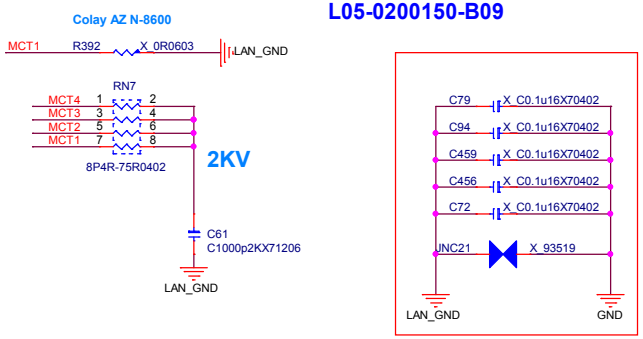
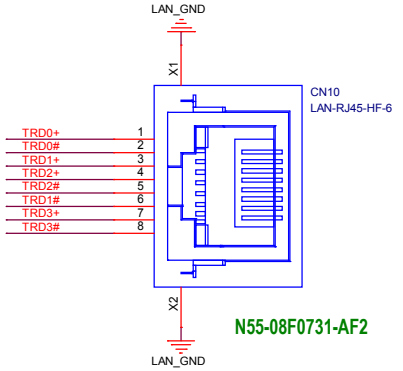
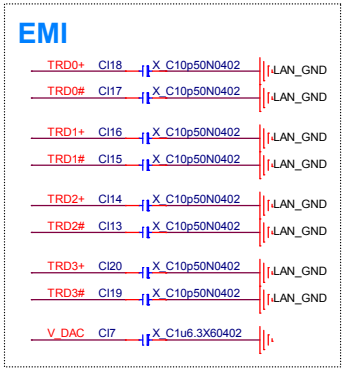




N55-08F0731-AF2



MICRO-STAR INT'L CO.,LTD.

Title: GIGA LAN(BigFoot BFN2205B)

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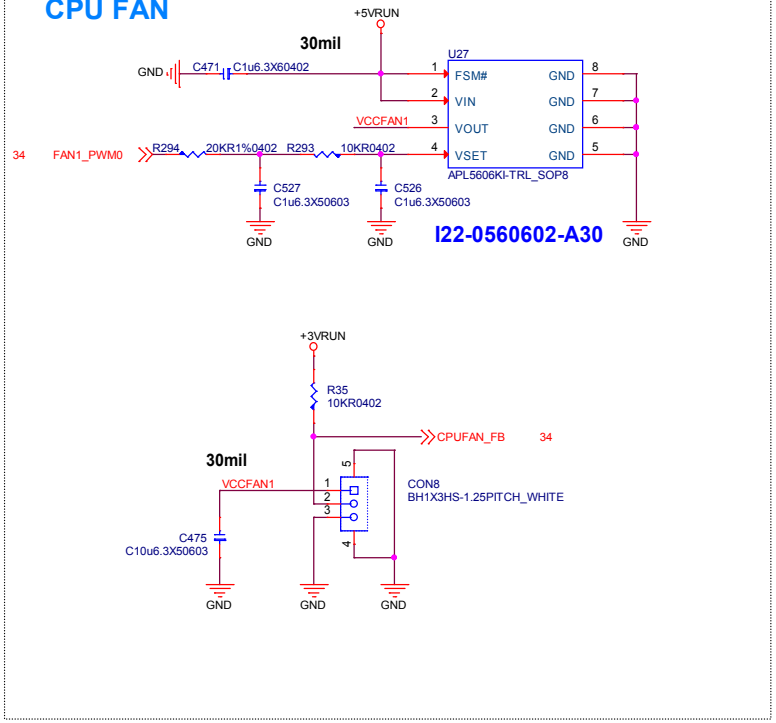
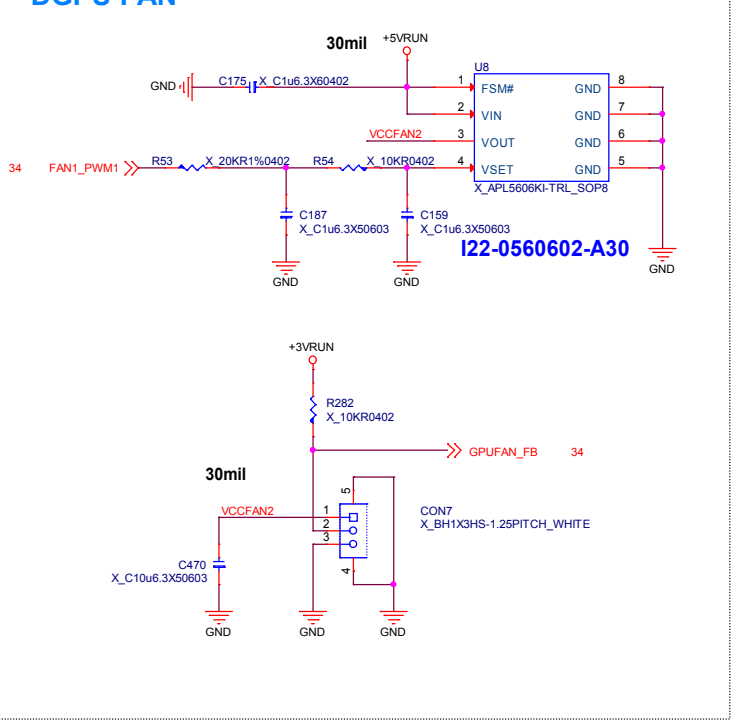
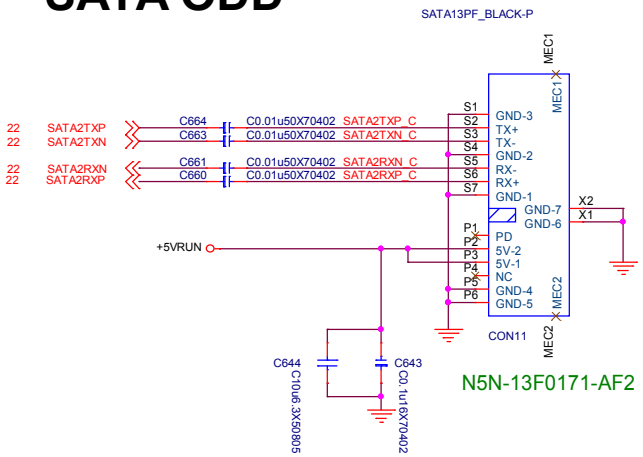
CPU FAN



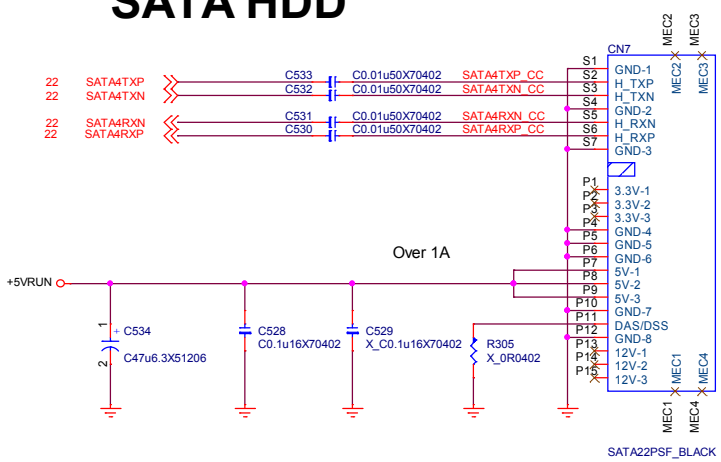
DGPU FAN



SATA ODD



SATA HDD



22.GND
21.TX
20.TX#
19.GND
18.RX#
17.RX
16.GND

15.V33
14.V33
13.V33
12.GND
11.GND
10.GND
9.V5
8.V5
7.V5
6.GND
5.Reserved
4.GND
3.V12
2.V12
1.V12

Title		
Size A3	ODD/HDD/FAN	Rev 1.0
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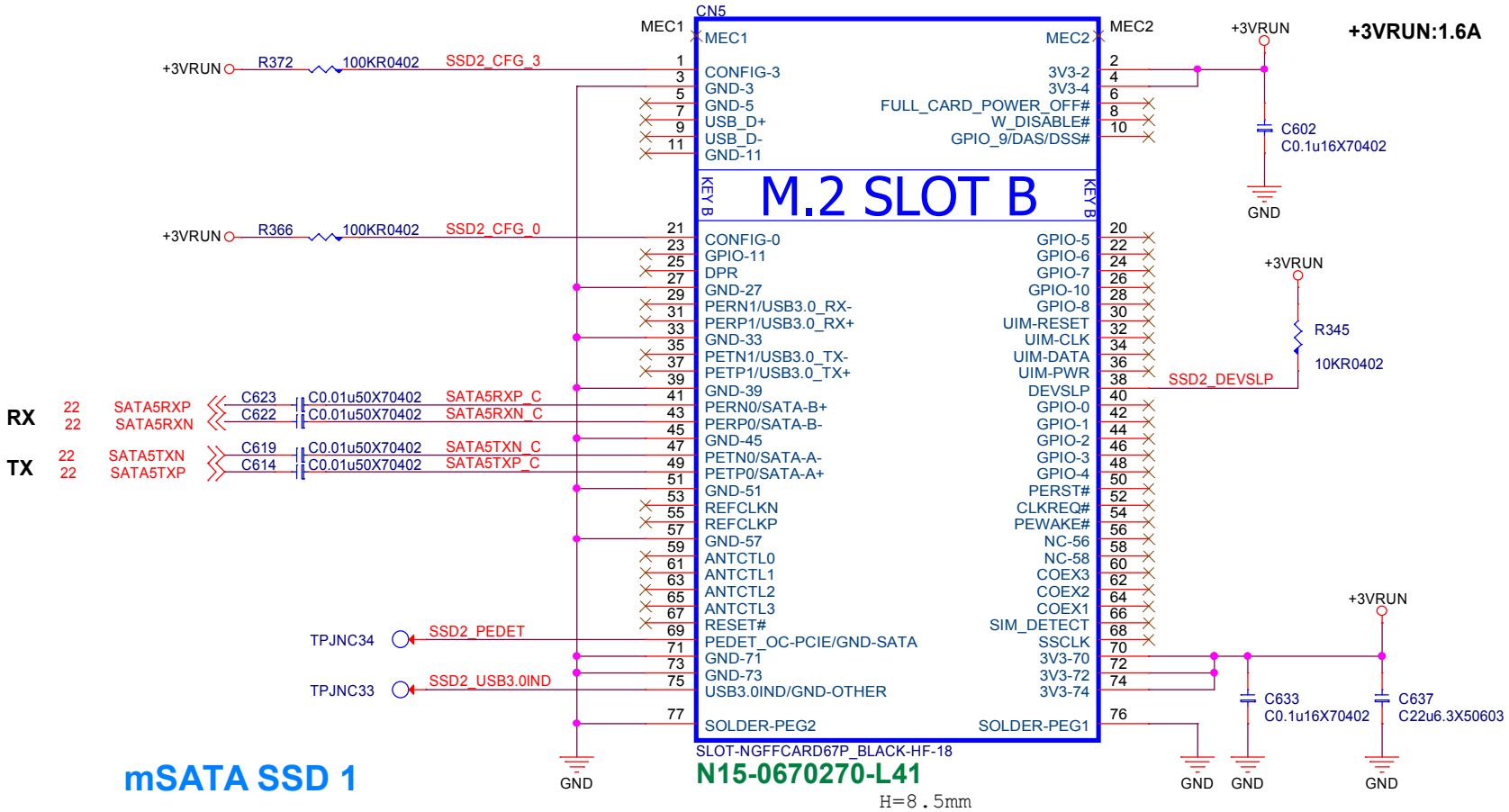
SSD



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	SSD		
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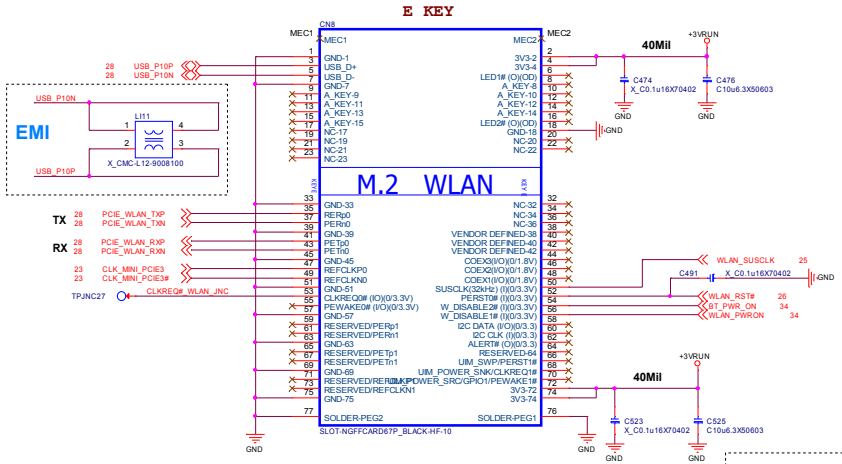
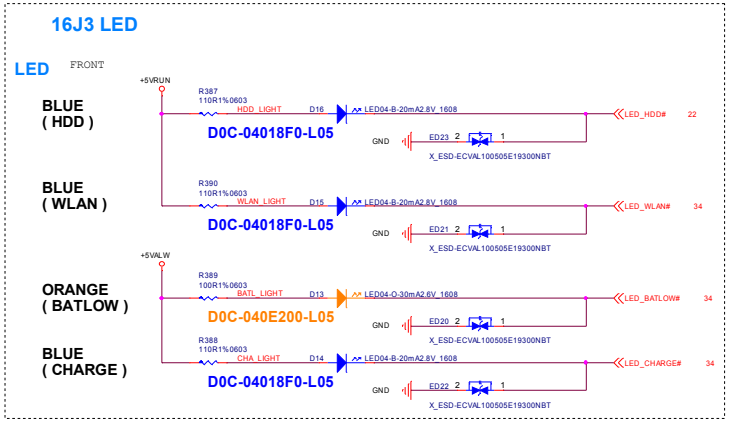
WLAN

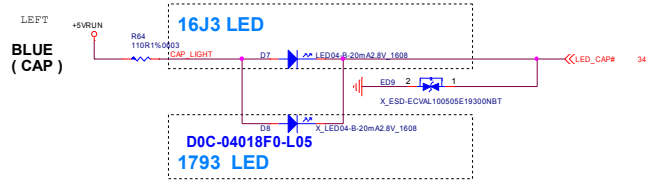
WLAN/LED



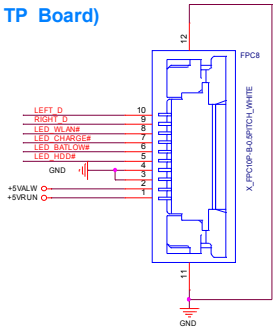
Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

16J3 LED

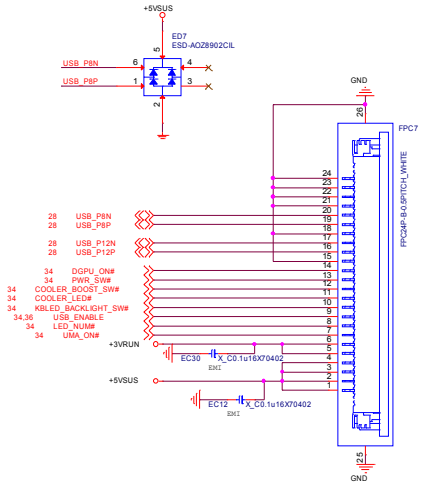




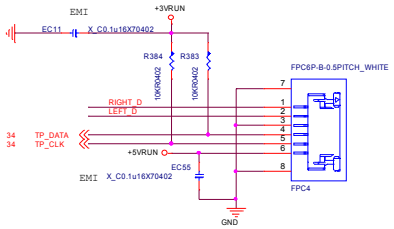
To 1793B (LED / TP Board)



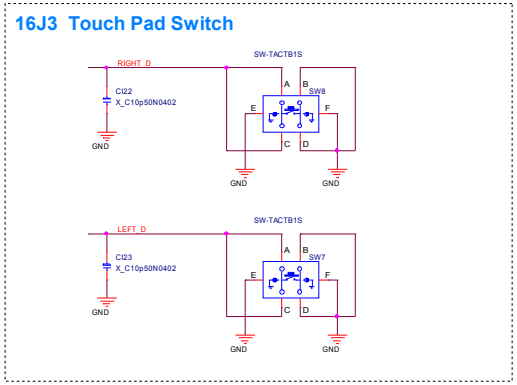
To 16J12 (Power Board/USB2.0/Card Reader Board)



Touch Pad



16J3 Touch Pad Switch



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MICRO-STAR INT'L CO.,LTD.			
Title	WLAN /LED/TP		
Size	Document Number		Rev
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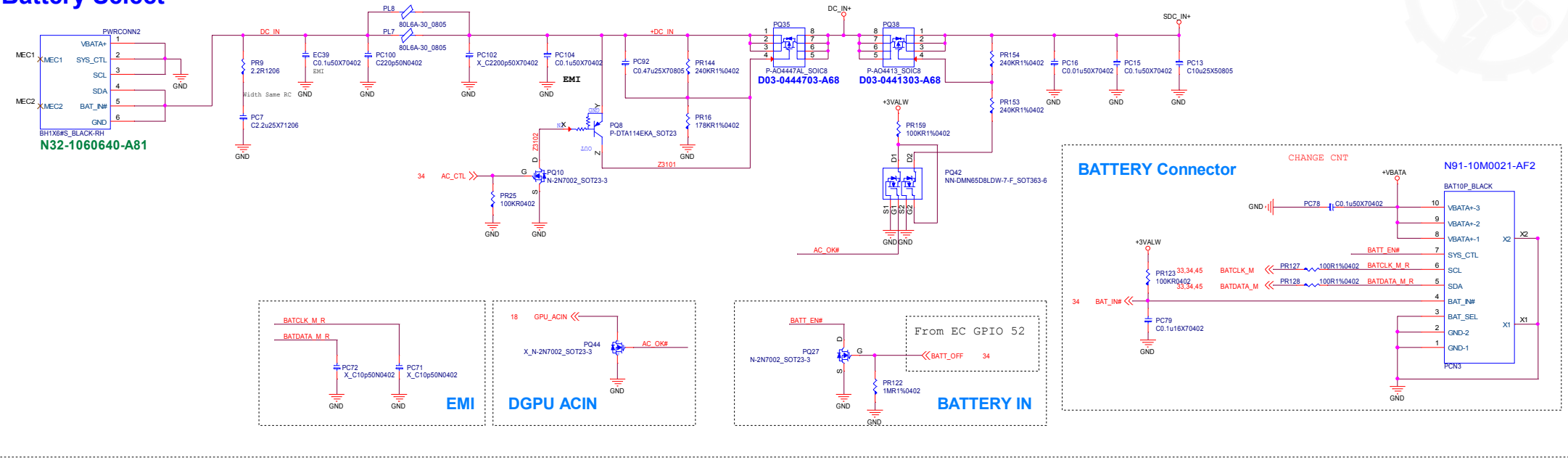
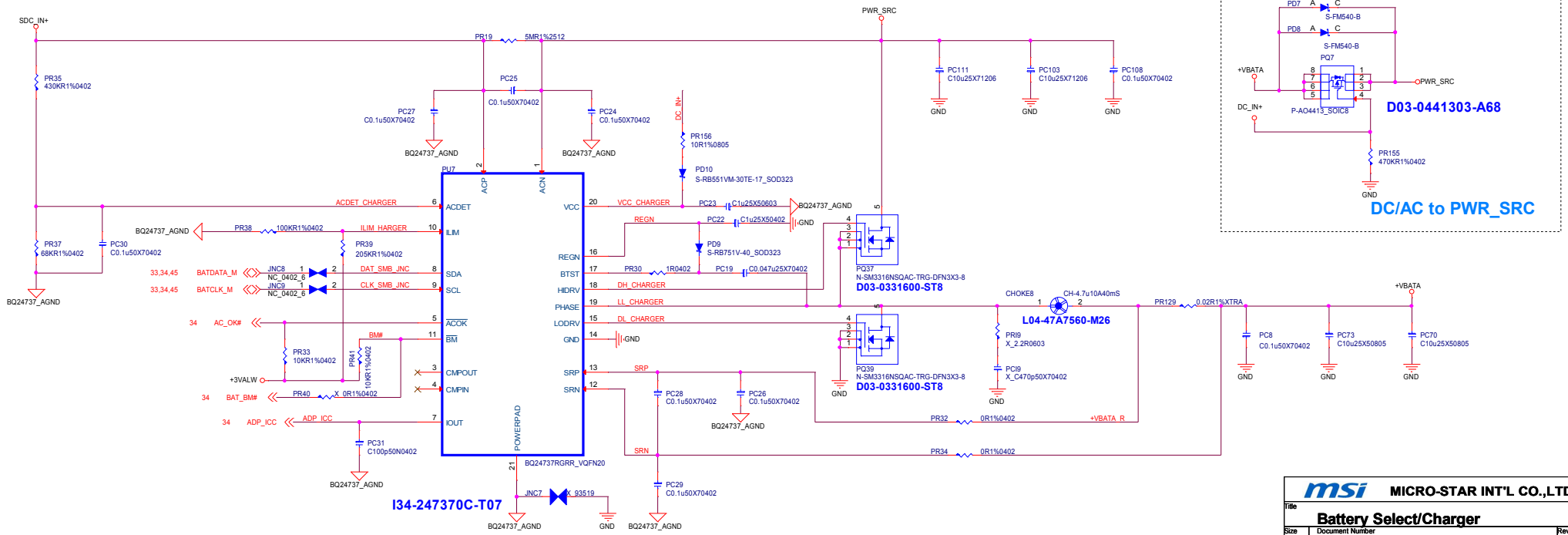
Battery Select/Charger

Battery Select



Battery Charger



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MICRO-STAR INT'L CO.,LTD.

Title: Battery Select/Charger

Size: Document Number: MS-16J3 Rev: 1.0

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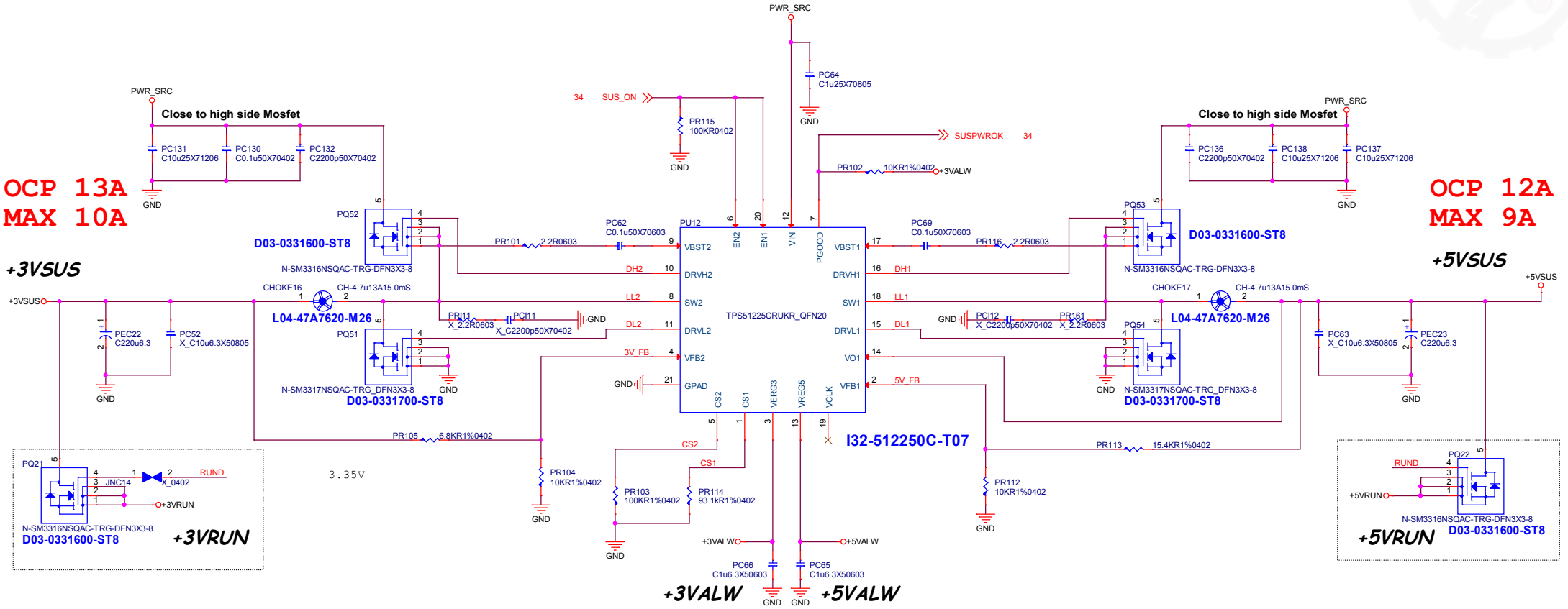
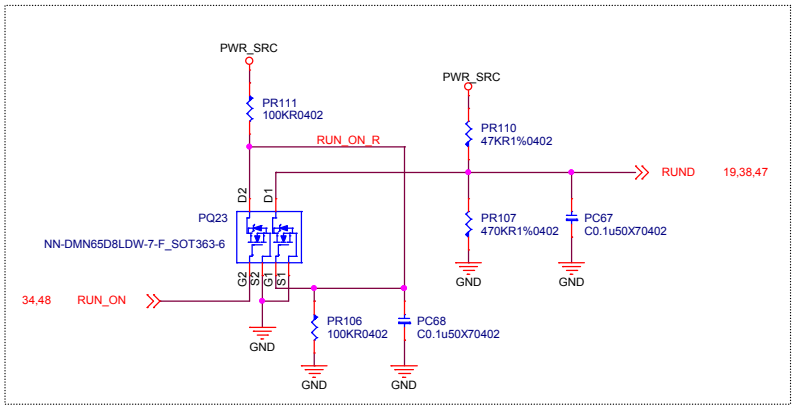
System Power





MICRO-STAR INT'L CO.,LTD.		
Title: System Power		
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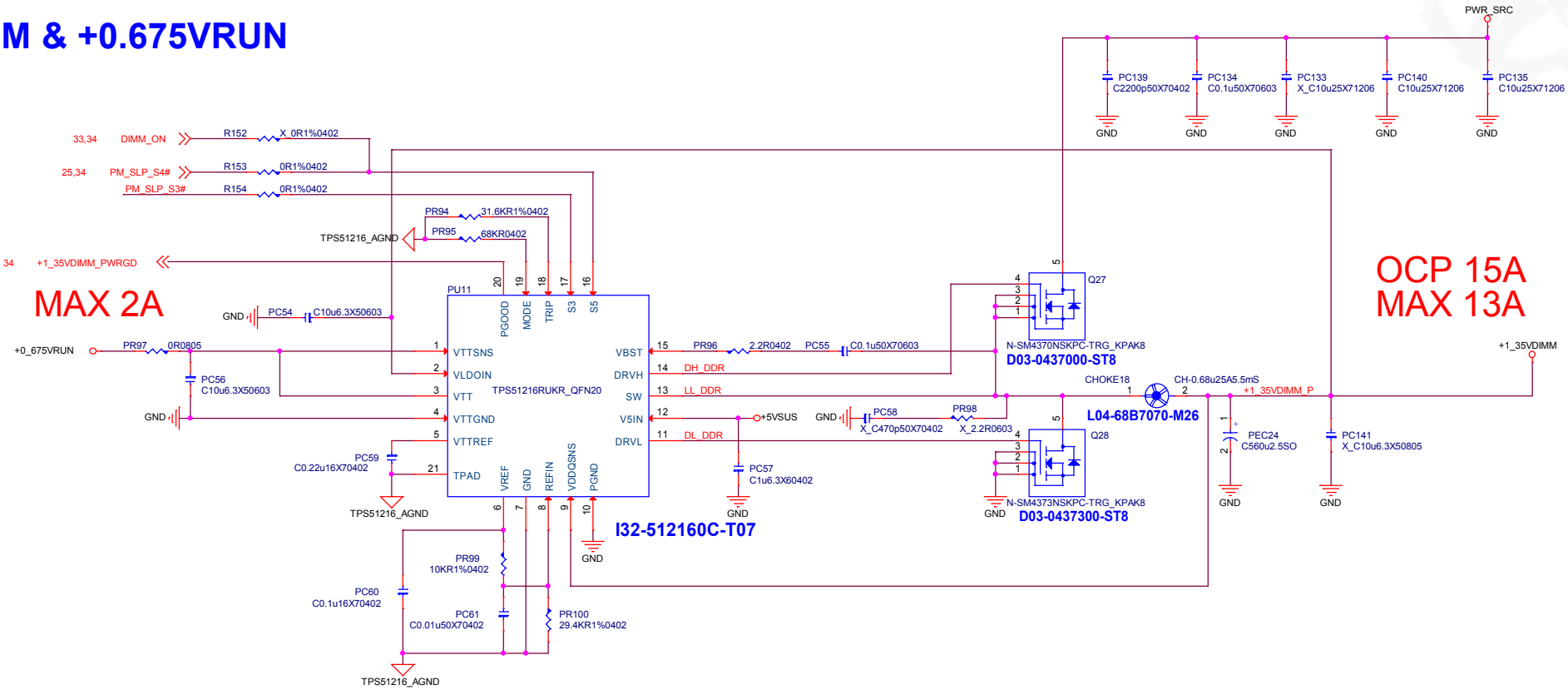
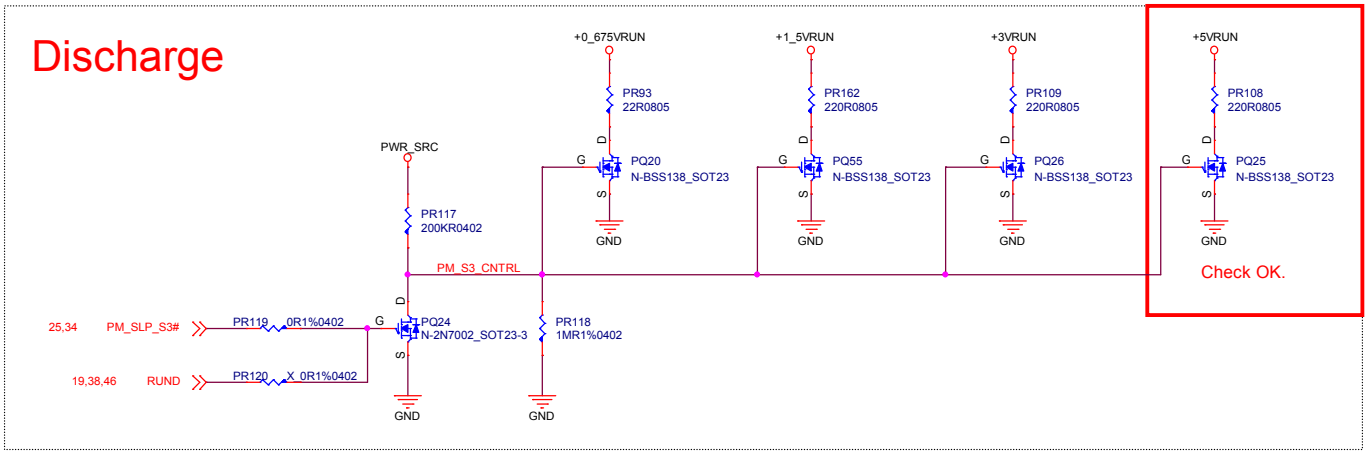
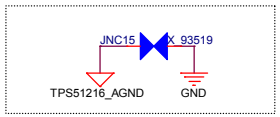
+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN







MICRO-STAR INT'L CO.,LTD.		
Title: +1.35VDIMM/+0.675VRUN		
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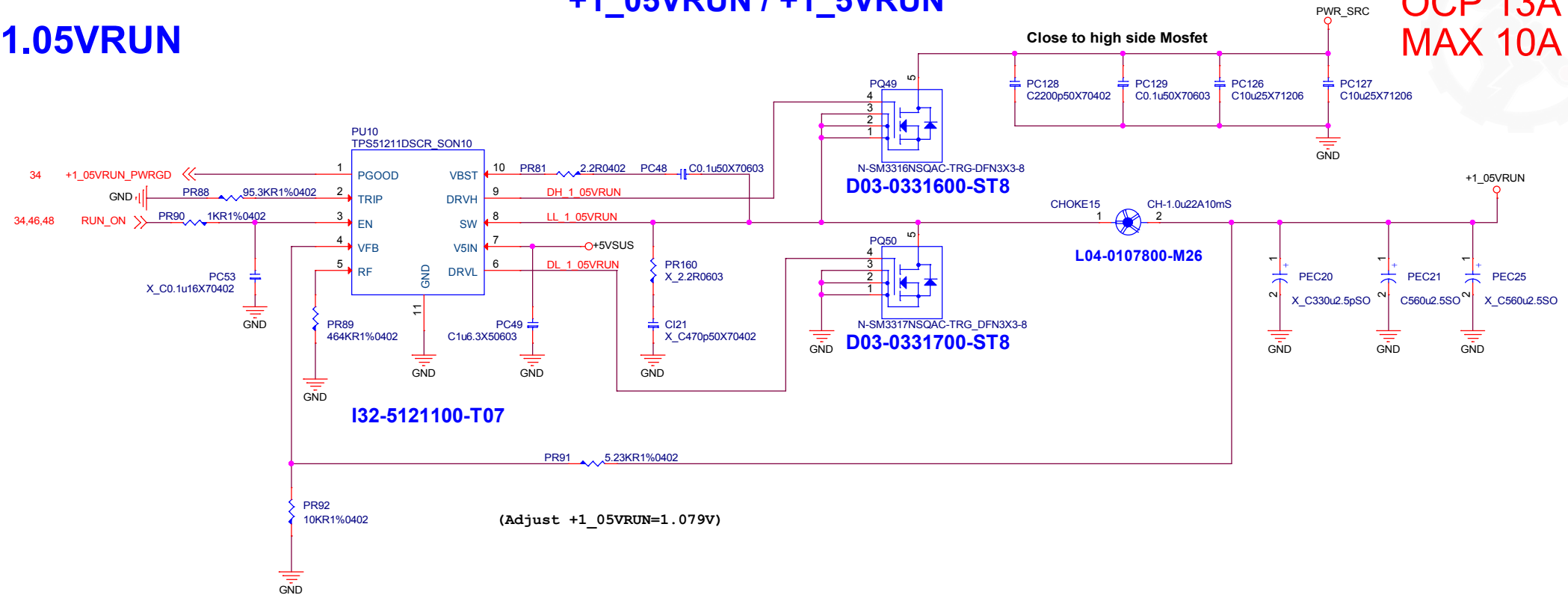
+1_05VRUN / +1_5VRUN

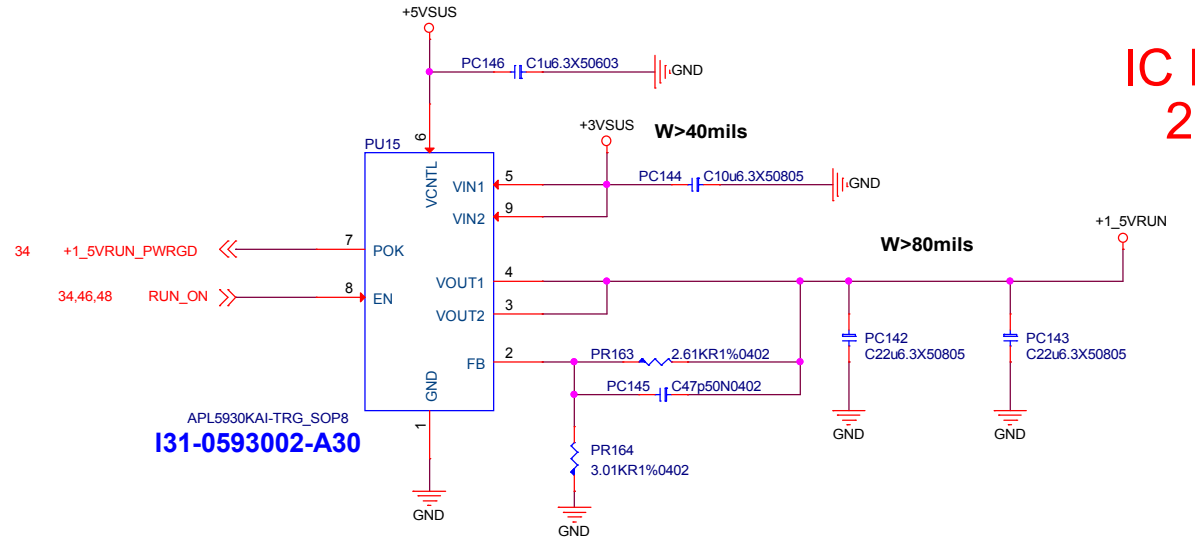
+1.05VRUN

OCP 13A
MAX 10A



+1.5VRUN

IC MAX 3A
253mA



MICRO-STAR INT'L CO.,LTD.

Title	+1_05VRUN / +1_5VRUN	
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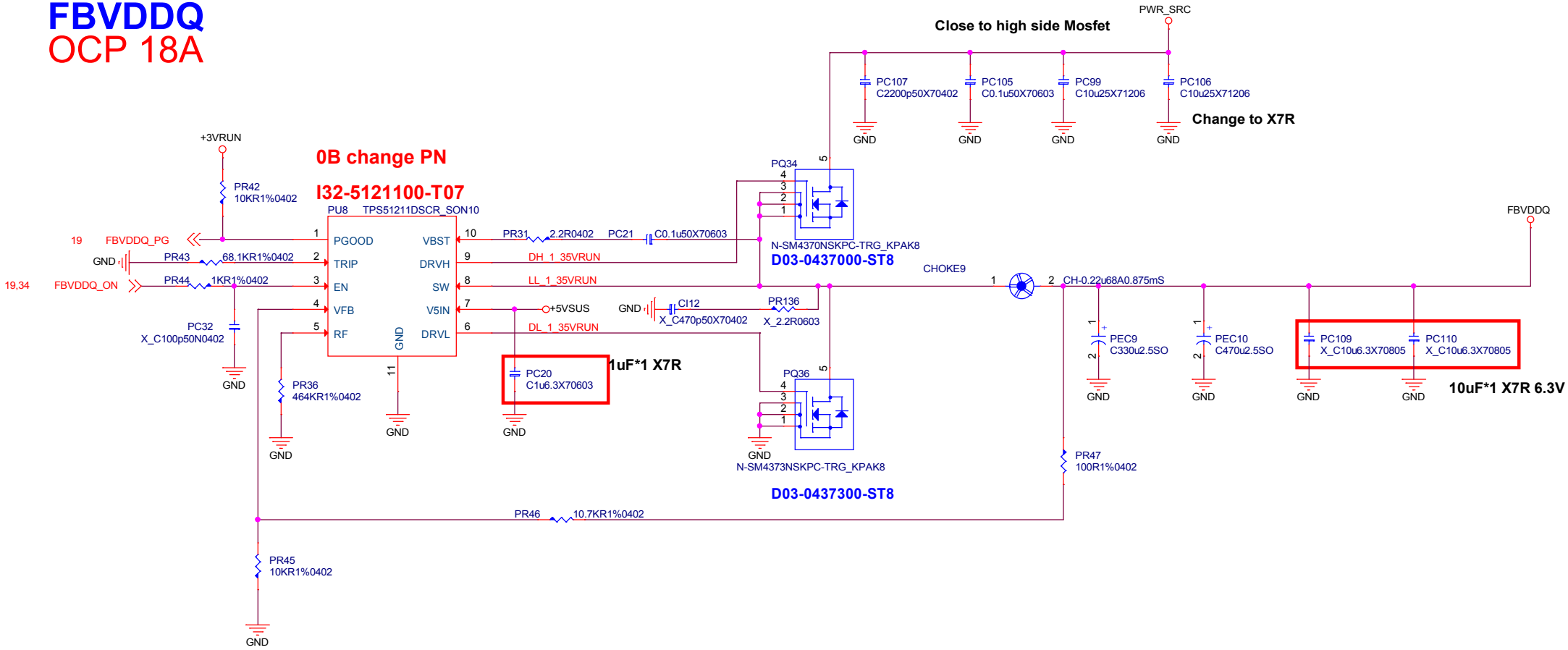
DGPU POWER FBVDDQ

FBVDDQ
OCP 18A



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU POWER FBVDDQ	
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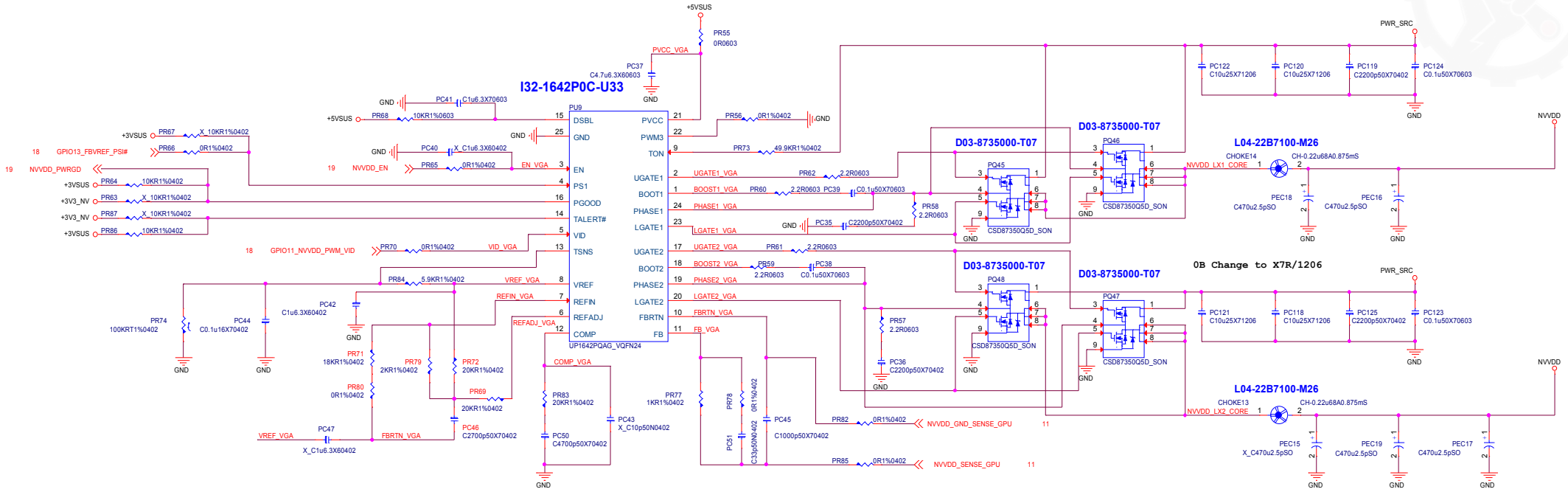
DGPU POWER / UP1642PQAG

EDP-Peak 70A

EDP-Con 50A

DGPU POWER NVVDD

CONFIG A
VBoot:0.875V
Vmin:0.6V / Vmax:1.2V



	PR56	PR52	PR53	PR54	PR121	PC45
CONFIG	R1	R2	R3	R4	R5	C
N16E-GT N16P-GX-B	20K	20K	2K	18K	0	2.7nF

20141029 power modify for GPU power setting
PR52,PR56: 39K ohm to 20K ohm
PR53: 1.5K ohm to 2K ohm
PR54: 30K ohm to 18K ohm
PR121: 1.5K ohm to 0 ohm
PC45: 1.5nF to 2.7nF

msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU POWER NVVDD		
Size	Document Number MS-16J3		Rev 1.0
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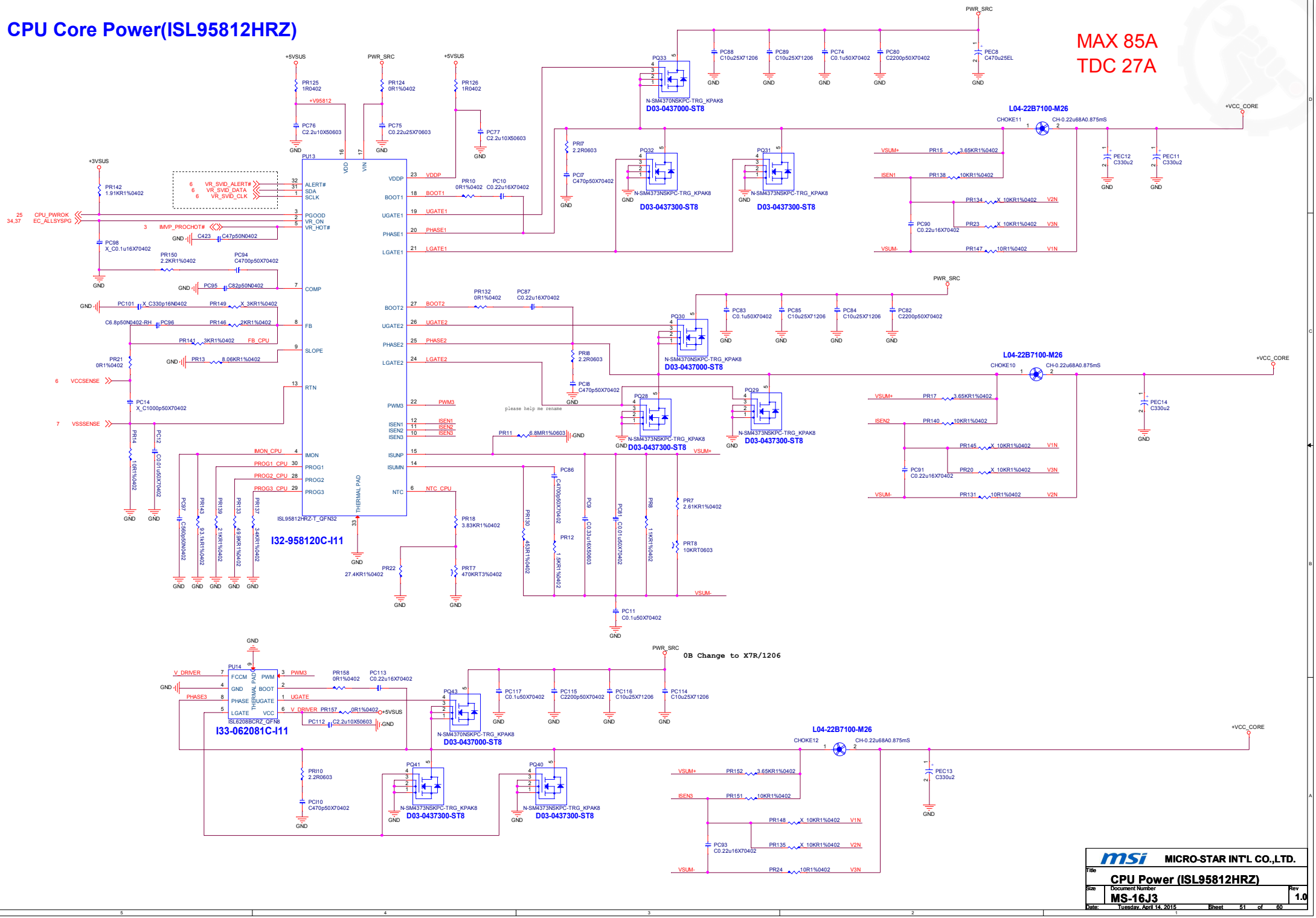
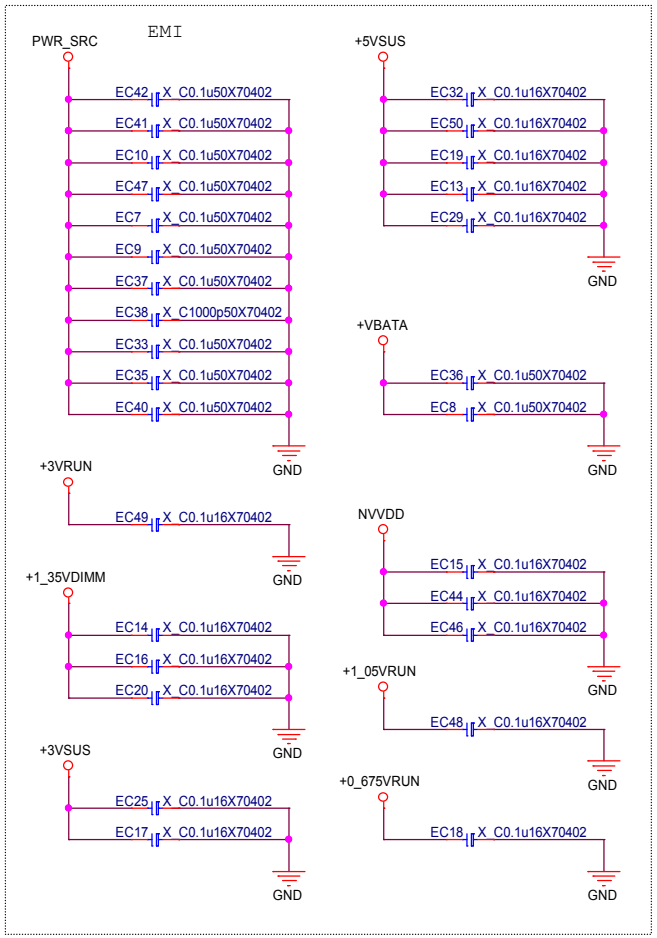
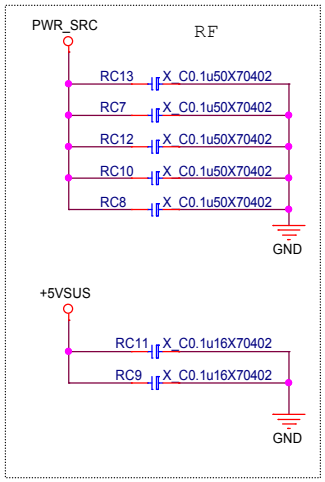
CPU Core Power(ISL95812HRZ)

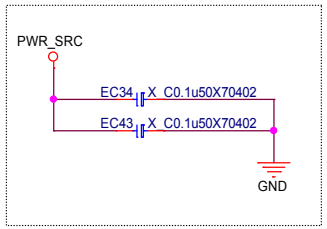
MAX 85A
TDC 27A



VINAFIX.COM







MICRO-STAR INT'L CO.,LTD.

Title: EMI/ Impedance

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CPU/GPU Holes

MCPU10 H_R276D169_PB
MCPU8 H_R276D169_PB
MCPU9 H_R276D169_PB
MCPU7 H_R276D169_PB
GND X_CPU_HOLE

MGPU9 H_R276D169_PB
MGPU7 H_R276D169_PB
MGPU8 H_R276D169_PB
MGPU10 H_R276D169_PB
GND X_GPU_HOLE

FM13 FM24 FM28 FM10 FM23 FM16 FM22 FM19
FM29 FM14 FM15 FM27 FM25 FM26 FM17 FM30
FM9 FM12 FM20 FM8 FM7 FM18 FM21 FM11
X_FM

MYLAR1 CPU MYLAR — CPU_MYLAR — E2P-6J11211-Y42
MYLAR2 HDMI/DP MYLAR — HDMI_DP_MYLAR — E2M-3570611-Y42
MYLAR3 USB3_CON_MYLAR — USB3_CON_MYLAR — E2M-3570611-Y42

CPU/GPU BRACKET

BRACKET1 CPU BKT — CPU_BRACKET — E2M-7810111-A89
BRACKET2 GPU BKT — GPU_BRACKET — 307-6G10311-A20

Only 16J3

MYLAR4 HIDE_GAP_MYLAR — HIDE_GAP_MYLAR — E2P-6J11411-Y42
MYLAR5 ME_MYLAR — Hide_Caps_Lock_LED_MYLAR — E2Y-6324111-Y42
SPONGE1 LED SPONGE — LED_SPONGE — E2Y-6J10611-Y42
SPONGE2 LED SPONGE — LED_SPONGE — E2Y-6J10611-Y42

HDD

SCREW1 E43-1205022-H29
SCREW2 E43-1205022-H29
SPONGE3 HDD SPONGE — HDD SPONGE — E2Y-6J10511-Y42

Only 1793

MYLAR6 MB MYLAR — X_MB MYLAR — E2P-7910311-G40
MYLAR7 MB MYLAR — X_MB MYLAR — E2P-0113511-G40
MYLAR8 MB MYLAR — X_MB MYLAR — E2P-7910811-G40
SPONGE4 LED SPONGE — X_LED_SPONGE — E2Y-7910211-G40

HOLE12 H_NR118D118_1 X_H_NR118D118_1
HOLE14 H_NR118D118_1 X_H_NR118D118_1
HOLE16 NPTH_80 X_NPTH_80
HOLE17 NPTH_80 X_NPTH_80
HOLE20 NPTH_80 X_NPTH_80
HOLE9 NPTH_80 X_NPTH_80
HOLE8 NPTH_80 X_NPTH_80
HOLE13 NPTH_80 X_NPTH_80
HOLE11 NPTH_80 X_NPTH_80
HOLE19 NPTH_80 X_NPTH_80
HOLE15 NPTH_80 X_NPTH_80
HOLE10 npth_98 X_npth_98
HOLE21 npth_98 X_npth_98
HOLE18 npth_98 X_npth_98
HOLE7 npth_98 X_npth_98
MH7 H_R197D118_PT X_ME_ SCREW HOLE — GND
MH9 H_R197D118_PT_V3 X_H_R197D118_PT_V3 — GND
MH8 H_R197D118_PT_V3 X_H_R197D118_PT_V3 — LAN_GND
MH14 HOLES_8X8_D3MM_VIA8 X_HOLES_8X8_D3MM_VIA8 — GND
MH10 H_R197D118_PT X_ME_ SCREW HOLE — GND
MH13 H_R197D118_PT X_ME_ SCREW HOLE — GND
MH12 H_R197D91 X_ME_ SCREW HOLE — GND
MH11 H_R197D91 X_ME_ SCREW HOLE — GND
MH15 H_R197D91 X_ME_ SCREW HOLE — GND

UME1 HDMI Lable — HDMI ROYALTY — Y01-RHDMI03-000
UME2 BIOS Lable — BIOS_LABEL — G51-LA01678-A09
PCB1 P30-16J3110-H73 — P30-16J3110-H73

Hannstar: P30-16J3110-H73
TRIPOD: P30-16J3110-T53

mSATA SSD 1 STAND OFF

H8 Spacer Support — SSD_STANDOFF H=8.5 — GND — E2B-1812010-A89

WLAN STAND OFF

H7 Spacer Support — SSD_STANDOFF H=4.15 — GND — E2B-16J1010-A89

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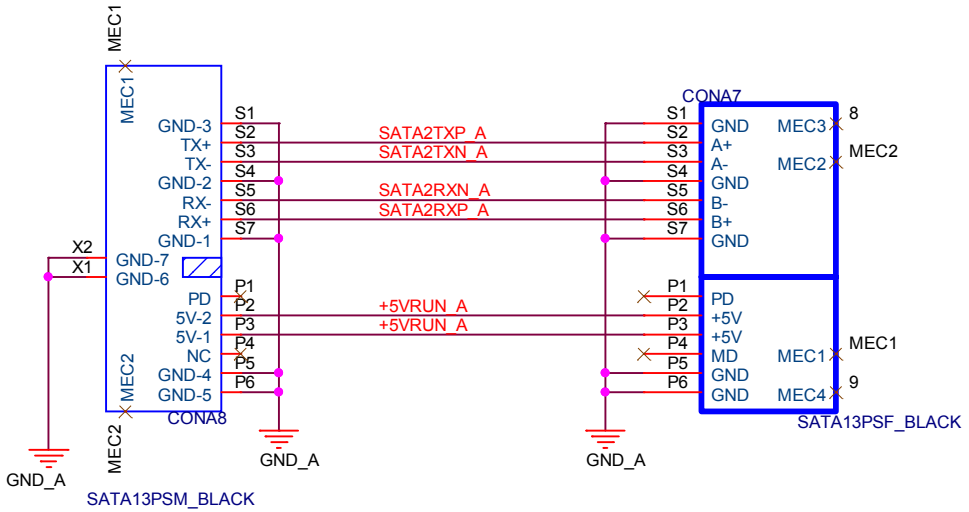
1793-A Board (ODD)



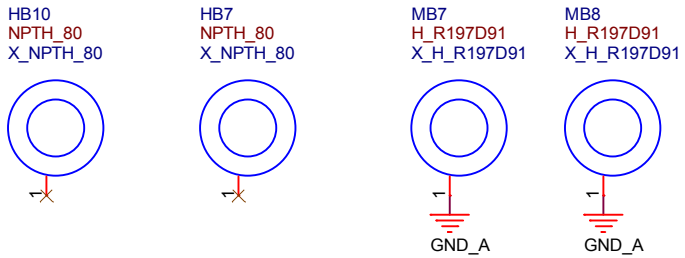
N5N-13M0060-AF2

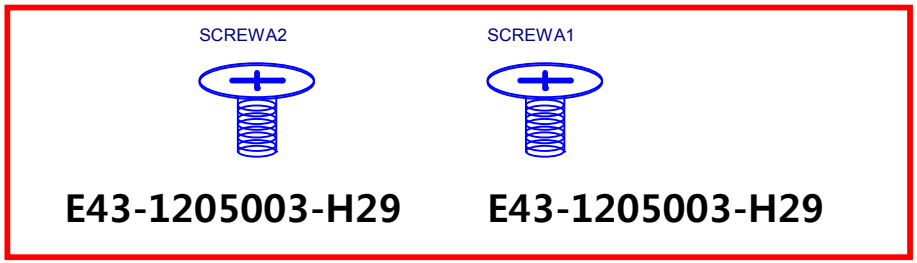
PCBA1

P30-16J3A10-H73

P30-16J3A10-H73

Hannstar: P30-16J3A10-H73
TRIPOD: P30-16J3A10-T53





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Title: [A] 1793 ODD

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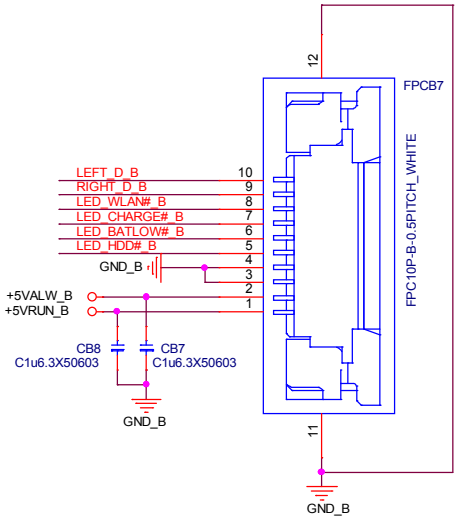
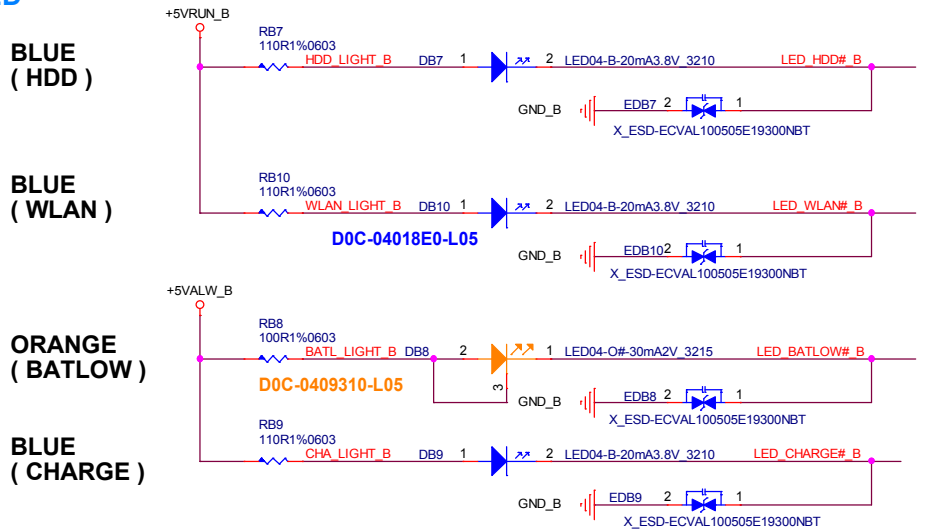
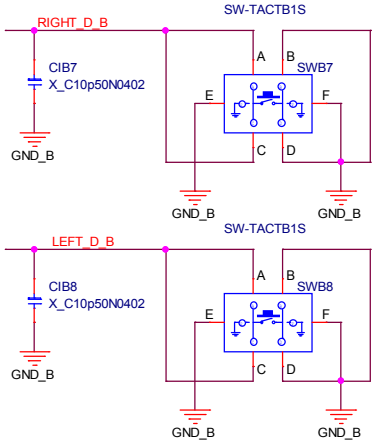
1793-B Board (LED / TP)



LED FRONT





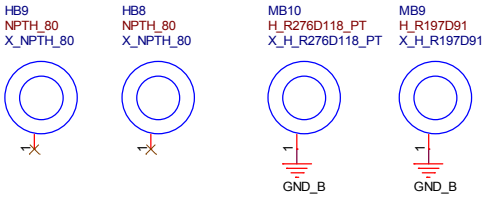
H=1.5mm

PCBB1

P30-16J3B10-H73

P30-16J3B10-H73

Hannstar: P30-16J3B10-H73
TRIPOD: P30-16J3B10-T53



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Title: [B] 1793 LED / TP

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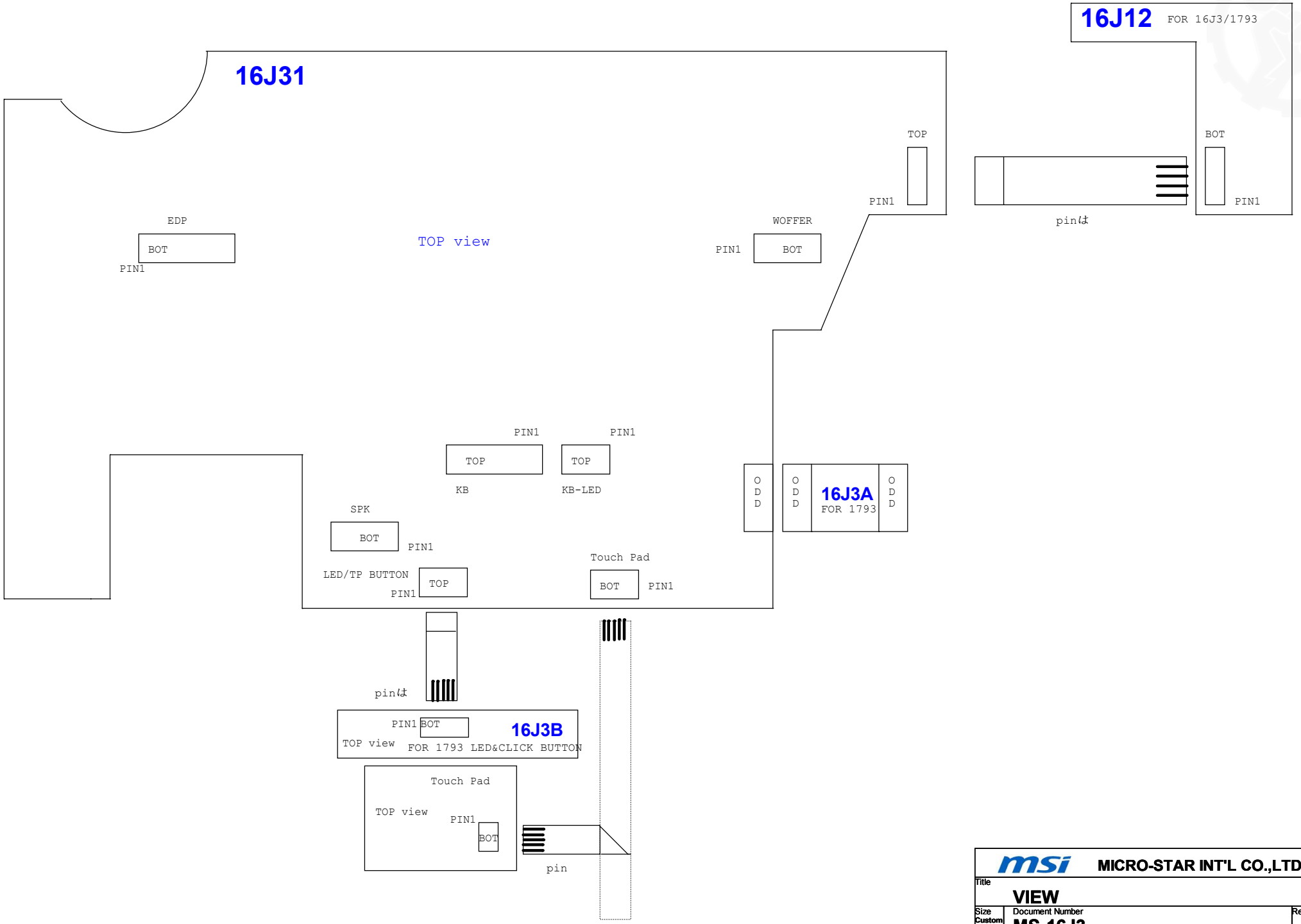

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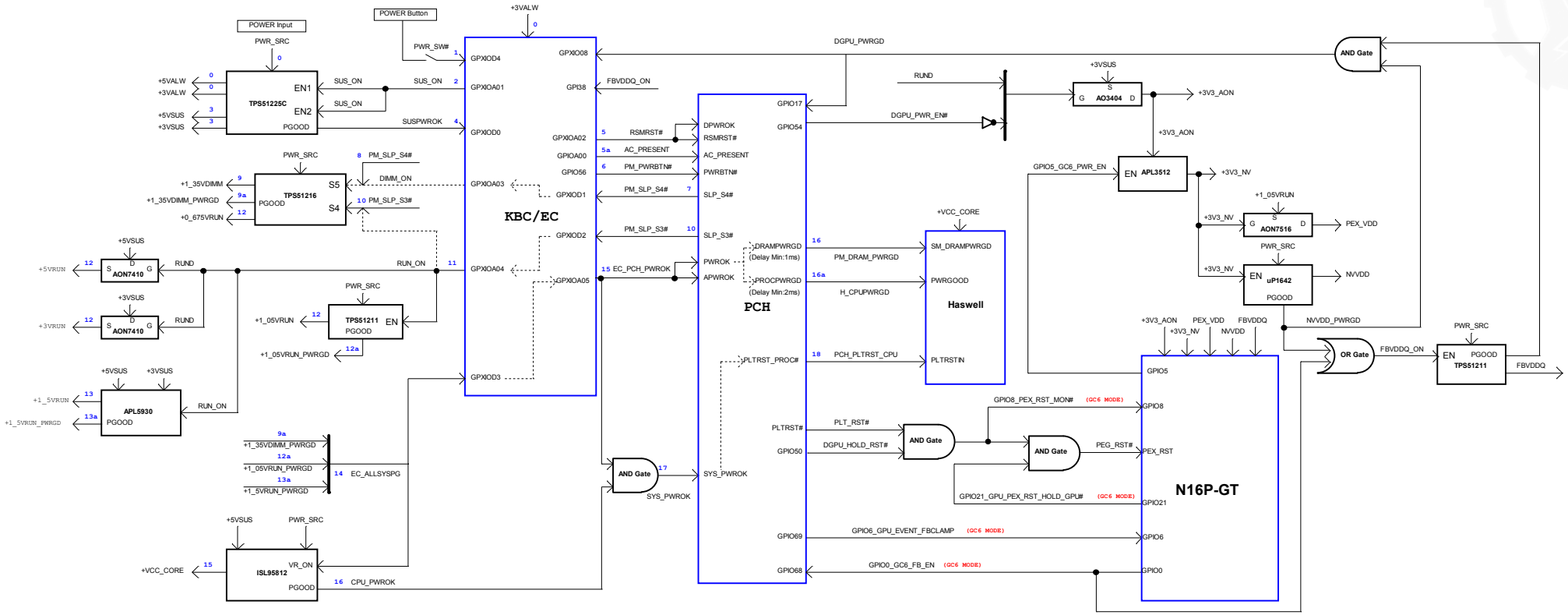
MS-16J3 Power on Block Diagram



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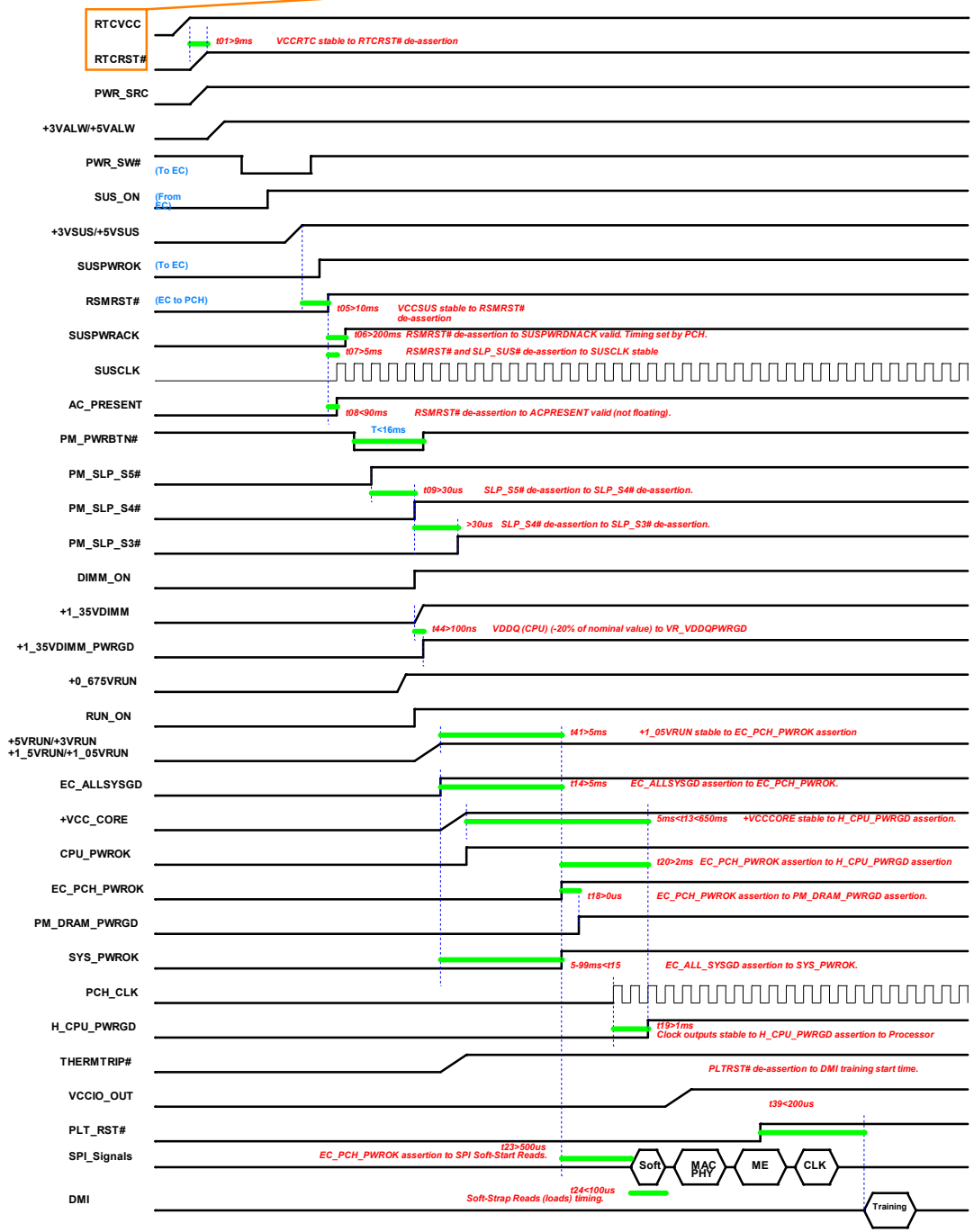
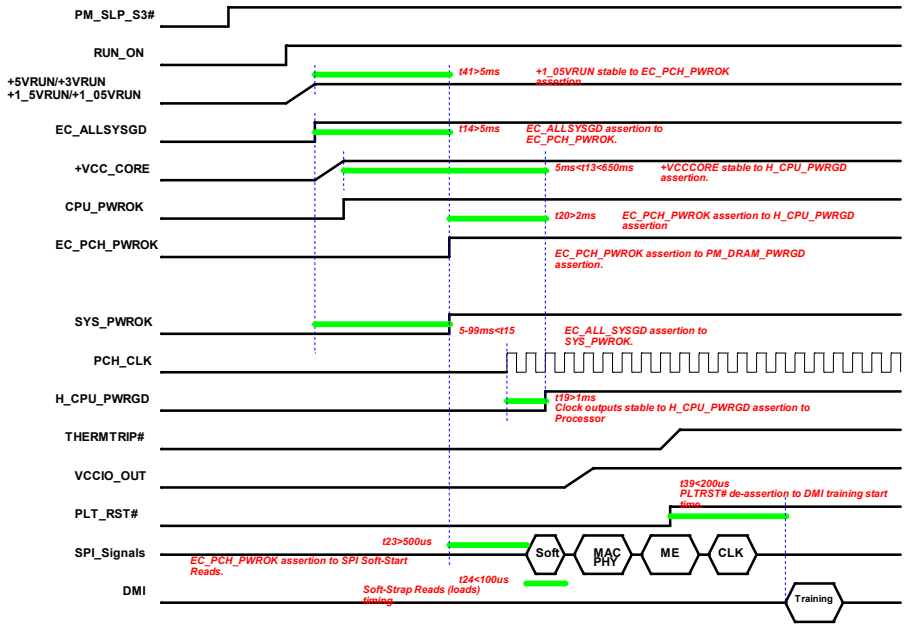
Power on Sequence

G3 -> S0



S3-> S0



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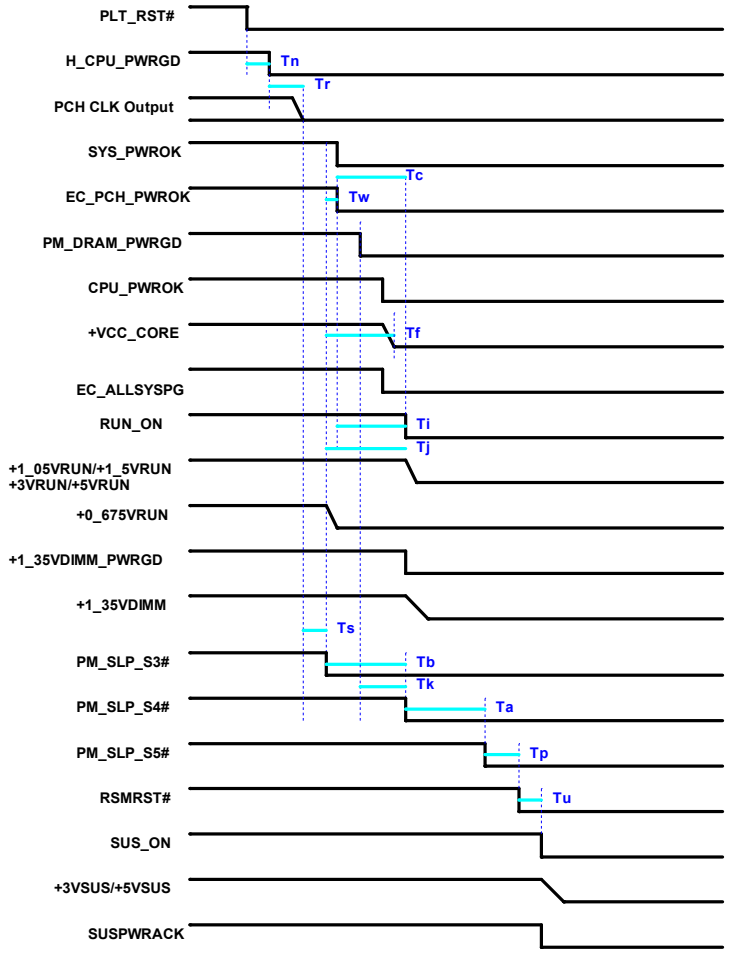
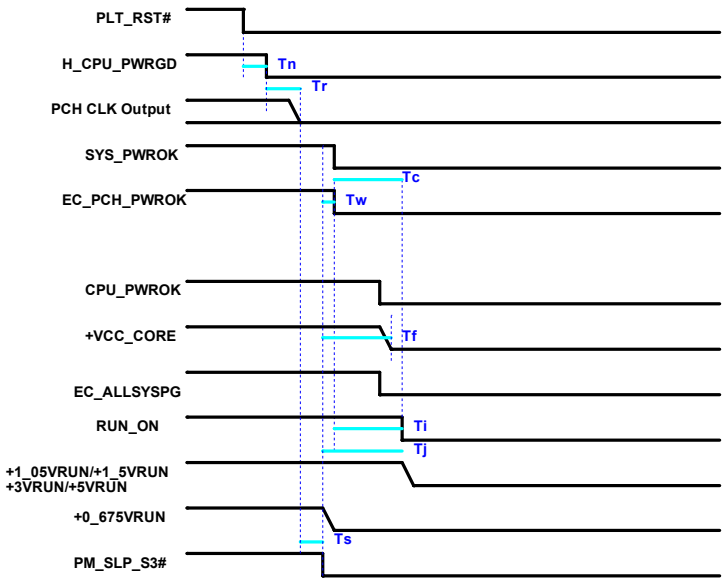
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3



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History

0A: 2014/12/24

01. P05 DEL TPJNC5
    DEL TPJNC4
    ADD R62 TO U68 PIN AB49
    ADD R63 TO U68 PIN V51

02. P26 ADD R293 TO DGPU_PWR_EN#
    ADD U18 R292 C495

03. P27 DEL R121
    DEL R204

2014/12/28

01. P05 CON3 N32-10200Q0-A81 change N91-02F0080-H06
    BAT1 D06-0105701-K26 change D06-0100101-K26

02. P36 DEL U29 U27 C669 C689
    ADD FR1 FR2
    C670 C71-101064G-S03 change C71-2210630-S03
    C687 C71-101064G-S03 change C71-2210630-S03
    ADD ED11 ED12 ED13 ED14 ED16

03. P44 ADD ED17

2014/12/29

01. P22 DEL SATA1TXP SATA1TXN SATA1RXP SATA1RXN
    DEL SATA0TXP SATA0TXN SATA0RXP SATA0RXN

02. P26 DEL R284

03. P28 DEL C437 C438 C436 C435 C433 C434
    DEL C432 C429 C427 C428

04. P35 DEL C42 C379 C381 C386 C387 C388 C389 C394 C401 C402
    C410 C412 C413 C414 C415 C416 C431 C673 C674 C675
    C675 C676 C677 C678 C679 C680 C682 C683 C684 C685
    C686
    DEL R151 R152 R154 R165 R167 R168 R169 R170 R173 R174
    R181 R182 R183 R186 R187 R189 R196 R201 R202 R209
    R210 R212 R217 R218
    DEL TPJNC8 TPJNC9 TPJNC10 TPJNC11
    DEL U9 U10 U11 Y1 CHOKE2

05. P36 DEL R178 R180 R397 R399 R172 R176
    DEL R177 R179 R398 R400 R171 R175
    DEL R185 R195 R408 R411 R198 R200
    DEL R184 R194 R409 R412 R197 R199

06. P38 ADD Q5 R86 C151

07. P43 DEL C472 C473 C476 C801 C802 C803 C804
    DEL R283 R475 R476
    DEL TPJNC41 TPJNC42
    DEL CN4
    DEL C461 C462 C463 C768 C777 C779 C788 EC41 EC42
    DEL R262 R277 R278 R446 R466 R468
    DEL TPJNC14 TPJNC16 JNC23
    DEL Q15
    DEL CN2
    DEL U31

2015/01/07

01. P18 ADD C7101

02. P32 R393 R392 0402 change 0603

02. P50 ADD PR60 PR76 PR123

2015/01/21

01. P50 DEL PEC5

2015/01/26

01. P36 DEL EL4 EL5 EL6 EL7 EL8 EL10

2015/01/28

01. P34 ADD C170

02. P49 DEL PQ20

2015/01/29

01. P50 DEL PR75 PR76

1.0: 2015/03/11

01. P36 C564 Footprint 100UF_16V_SMD_H6 change C_B_3528
    C572 Footprint 100UF_16V_SMD_H6 change C_B_3528

1.0: 2015/03/17

01. P19 ADD PR75 R391 PQ56 PC147

1.0: 2015/03/23

01. P9 ADD C673
02. P10 ADD C674

1.0: 2015/03/30

01. P32 ADD C675

1.0: 2015/04/07

01. P41 ADD R392

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